

Record Voltages using Commercial-grade Silicon Wafers: An Assessment of the Impacts of Defect Engineering for p-type Silicon Heterojunction Solar Cells

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The passivation qualities of hydrogenated amorphous silicon films (a-Si:H) have been studied extensively on silicon heterostructures since the 1970s [1]. With inherently low surface recombination velocities, these films have allowed for record open-circuit voltages (V_{OC}) of over 750 mV on finished devices in addition to record efficiencies beyond 26% [2]. Another attributed advantage of such these silicon heterojunction (SHJ) devices is the low temperature required for fabrication which helps prevent bulk degradation associated with high temperature treatments. Although this may be beneficial for maintaining film quality, lower temperatures inhibit the use of lower quality wafers which usually require elevated temperature treatments such as gettering or hydrogenation to raise bulk performance. It is, therefore, no surprise that silicon heterojunction devices are commonly fabricated on expensive, high-quality n-type Czochralski-grown and/or Float zoned silicon wafers. In our previous work, we demonstrated the use of pre-fabrication hydrogenation and gettering treatments to improve the quality of p-type Cz silicon wafers prior to SHJ cell fabrication [3].

In this work, we investigate the impact of these processes on both p-type Cz and multicrystalline (mc-Si) silicon wafers and analyse the effect of gettering on interstitial iron concentrations ($[Fe_i]$) in addition to the mitigation of boron-oxygen (BO) related light induced degradation (LID) through hydrogenation. For gettering pre-treatments, wafers undergo a heavy phosphorus diffusion (65 Ω /sq) followed by a texturing etch to remove gettered impurities. Bulk hydrogenation and passivation defects is then achieved by depositing industrial silicon nitride ($SiN_x:H$) films on both sides followed by a high temperature firing step. These films are subsequently stripped off in preparation for SHJ fabrication. The results in Fig 1. demonstrate that gettering alone can facilitate the removal of over 2 orders of magnitude of $[Fe_i]$ from the silicon wafer, from $[Fe_i] = 3 \times 10^{11} \text{ cm}^{-3}$ down to below $1 \times 10^{10} \text{ cm}^{-3}$ (Fig.1 (a)). The application of both gettering and hydrogenation in conjunction with each other results in nearly 7-fold increases in the bulk minority carrier lifetime, corresponding in an 80 mV enhancement in the average measured iV_{OC} (Fig 1. (b,c)).

In Figure 2, photoluminescence imaging shows the influence of gettering and hydrogenation on the removal of bulk defects and impurities from within mc-Si wafers. We demonstrate that hydrogenation and gettering alone only results in slight improvements of the intra-grain regions and do not facilitate the passivation of crystallographic defects such as grain boundaries. The combination of both processes however, results in a clear reduction in the recombination activity from within grain boundaries in addition to an enhancement of the intra-grain regions. In the final presentation, we will demonstrate that these processes are also highly effective on n-type mc-Si wafers; which are usually already of a much higher quality than its p-type counterpart.

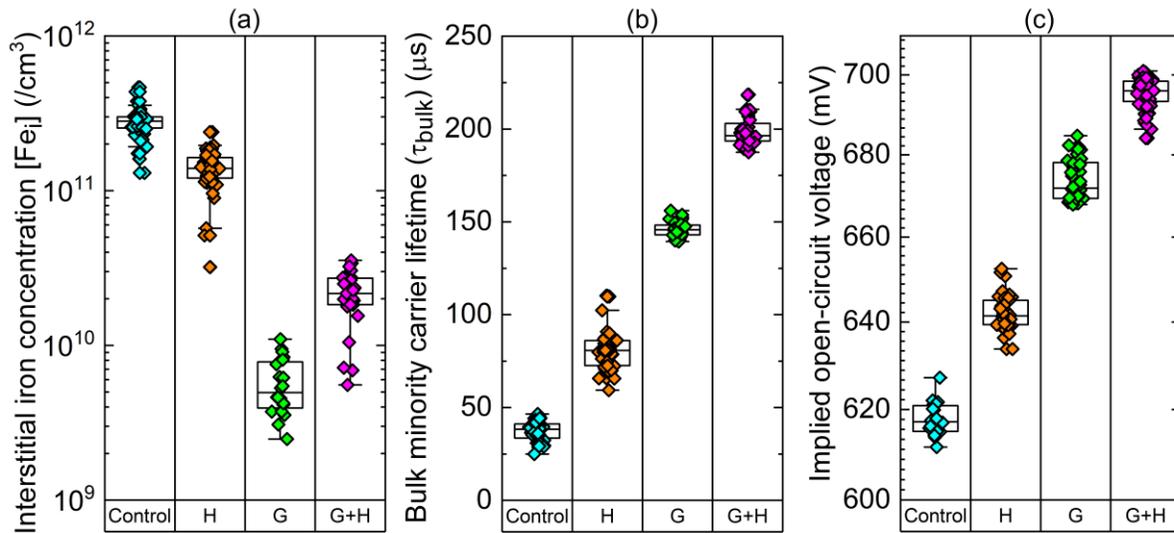


Figure 1. a) Interstitial iron concentrations, b) bulk minority carrier lifetimes and c) iV_{OC} measured on $SiN_x:H$ passivated Cz samples from various defect engineering process groups.

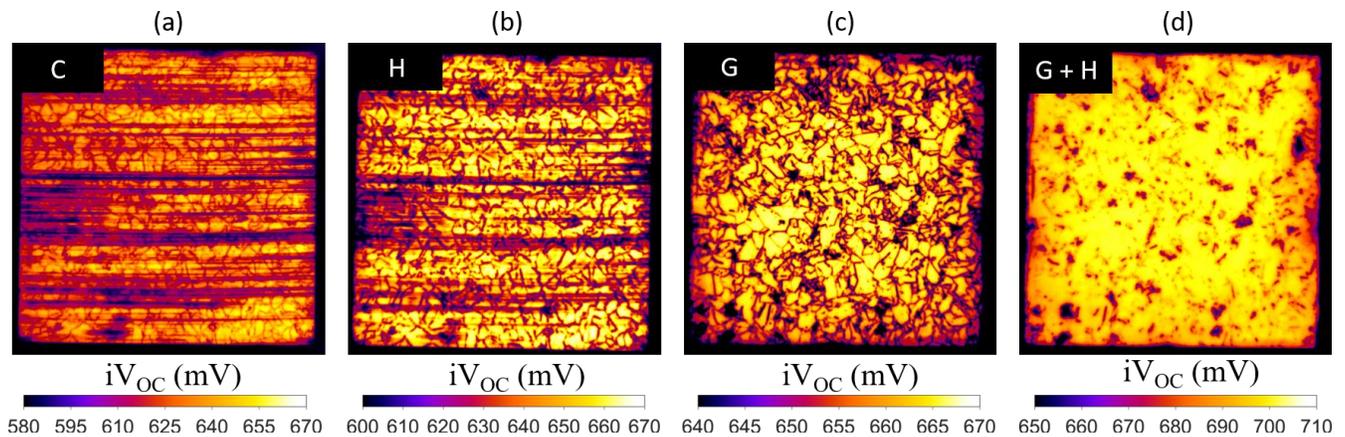


Figure 2. iV_{OC} calibrated photoluminescence images of mc-Si silicon wafers after various defect engineering treatments.

On finished SHJ solar cells, we were able to then demonstrate independently verified, record open-circuit voltages of 707 mV and 702 mV on Cz and mc-Si materials respectively. In the final presentation, we will show further results on silicon heterojunction solar cells, mitigation of the BO defects and planned experiments to further boost the performance of lower quality silicon wafers.

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2. Yoshikawa, K., Yoshida, W., Irie, T., Kawasaki, H., Konishi, K., Ishibashi, H., Asatani, T., Adachi, D., Kanematsu, M., Uzu, H., and Yamamoto, K. (2017) Exceeding conversion efficiency of 26% by heterojunction interdigitated back contact solar cell with thin film Si technology. *Sol. Energy Mater. Sol. Cells*, **173** (April), 37–42.
3. Hallam, B., Chen, D., Shi, J., Einhaus, R., Holman, Z.C., and Wenham, S. (2018) Pre-Fabrication Gettering and Hydrogenation Treatments for Silicon Heterojunction Solar Cells: A Possible Path to >700 mV Open-Circuit Voltages Using Low-Lifetime Commercial-Grade p-Type Czochralski Silicon. *Sol. RRL*, **2** (2), 1700221.