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SHAOYANG LIU

Exploring the Potential and Limitations of Interdigitated Back Contact Solar Cells Using Experimentally Validated Quokka 3-D Simulation

Shaoyang Liu[1], Michael Pollard[1], David N.R. Payne[1], Alexander To[1], Bram Hoex[1], Catherine Chan[1], Stuart Wenham[1], Darren M. Bagnall[1]

[1]UNSW Australia, School of Photovoltaic and Renewable Energy Engineering, Sydney, N.S.W. 2052 Australia
E-mail: shaoyang.liu@student.unsw.edu.au

Abstract

Interdigitated back contact (IBC) designs feature no optical shading loss at the front surface and have the potential to reach relatively high efficiencies with the current world record of 26.33% for a silicon cell achieved using an IBC design with silicon heterojunction (SHJ) contacts. However, the IBC design presents several challenges, such as the need for excellent front surface passivation, carrier transport and material quality. The requirement for fine contact patterns on the back side of the device leads to increased fabrication complexity and this is a barrier to wide-spread adoption of IBC technology by the photovoltaic industry. One possible approach to improving the competitiveness of the technology would be to move towards thinner substrates as this will result in a reduction in the required minority carrier diffusion lengths and an increase in open circuit voltages. Another option is to move away from expensive *n*-type substrates and towards the development of an IBC technology on *p*-type wafers. Whilst *p*-type wafers historically have much shorter minority carrier diffusion length than *n*-type, recent advances in low-cost material processing, such as advanced hydrogenation techniques, have helped to drive these lifetime values closer to those achievable in *n*-type. In this work, we explore the limitations and potential of IBC based cell designs for realistic *n*- and *p*-type material parameters over a range of substrate thicknesses. This analysis is carried out using 3-D Quokka simulations and validated by experimental results acquired from the ongoing development of a planar *n*-type IBC baseline at UNSW. This baseline is currently achieving efficiencies of up to 18.7 % with a V_{OC} of 677 mV, J_{SC} of 37.4 mA/cm^2, and *FF* of 74%. For the *n*-type device, simulation-based optimisation reveals that open circuit voltages of up to 725 mV could be achieved with a planar front surface while up to 727 mV could be achieved with pyramidal texturing. Simulations also suggest that an efficiency exceeding 20% could be achieved for *p*-type planar IBC cells with this expected to increase to 22% for conventionally planar devices and up to 24.73% with a V_{OC} of 729 mV, J_{SC} of 41.65 mA/cm^2, and *FF* of 81% if more advanced light trapping schemes (random upright pyramids texturing or nanophotonic) can be efficiently incorporated.

1. Introduction

Since the concept of the interdigitated back contact (IBC) solar cell was proposed by Schwartz and Lammert in the 1970s (Lammert & Schwartz 1977), IBC solar cell designs have attracted much attention, leading to ongoing mass production and broad acknowledgement as an outstanding design choice for achieving world record efficiencies (Smith et al. 2014)(Masuko et al. 2014). The lack of metallic contacts on the front surface eliminates optical shading, thereby offering the potential for increased short circuit current densities, J_{SC} (Lu et al. 2009). However, electrical shading is introduced due to large lateral dimensions on the rear of the device. Moreover, compared with standard front grid solar cells, by putting all contacts on the back side of the device, IBC solar cells do not require front-to-rear interconnections, therefore allowing maximized module packing density.

However, under normal solar irradiance, the majority of electron-hole pairs are generated near the front surface (< 30μm) of the IBC solar cell (Lu et al. 2007). Minority carriers therefore need to diffuse through the device thickness in order to be collected by the contacts at the back of the IBC solar cell. This requires a higher minority carrier lifetime in the bulk (τ_{bulk}) of the device to enable a large diffusion length. Traditional *p*-type Cz silicon wafers suffer carrier induced degradation caused by boron-oxygen defects resulting in much lower carrier lifetimes in comparison with *n*-type wafers. Recent studies have demonstrated that hydrogen passivation can permanently deactivate these boron oxygen defects, transforming them into a recombination inactive state and thus improving the minority lifetime, with minority carrier diffusivity achieved approximately three times higher compared with *n*-type in the literature (Walter & Schmidt 2016). Another possible solution to circumvent the typically low carrier lifetime in *p*-type IBC solar cells is to fabricate with thinner substrates, therefore reducing the minority carrier diffusion length required.

To investigate the limitations and true potential of both *n*- and *p*-type IBC designs over a range of substrate thicknesses, the free solar cell modelling software 'Quokka' was used (Fell 2013). In comparison with other commercial simulation tools such as ATLAS, Quokka has been proven to be capable of producing results of a similar accuracy (Fell et al. 2014). The file setting generator with simple step-by-step instructions can be found on 'PVlighthouse', allowing for straightforward and efficient modelling of cells. In order to simulate IBC silicon solar cell designs in Quokka, several material parameters must be specified, including the recombination current prefactor, J_0, for the various regions of the solar cell which is a key parameter indicating the quality of the contacts, bulk, and surface region.

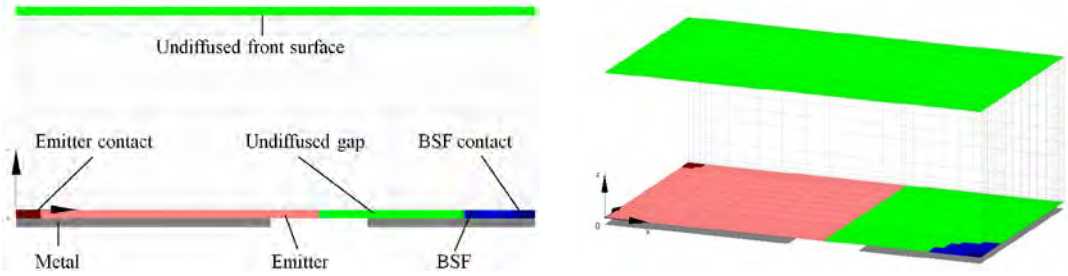
2. Three-Dimensional (3-D) Modelling Details and Parameters

The baseline unit-cell model for an IBC solar cell with planar front surface is shown in Figure 1. The cell design to be modelled utilizes point contacts, so it is necessary to use a 3-D simulation. The cell structure and material parameters are either chosen based on direct measurement results, test structures or from realistic values reported in the literature.

UNSW Australia is currently developing an *n*-type planar baseline IBC solar cell for the initial purpose of testing proof-of-concept nanophotonic light trapping schemes. To date, the best cell produced has an efficiency of 18.7% with aperture (3.06 cm^2) illumination. The initial model setup was based on this fabricated cell for a 2Ωcm *n*-type wafer with a thickness of 280μm. The front surface geometry and photogenerated current generation profile as a function of cell depth was determined using a generation calculator, namely OPAL 2

(McIntosh & Baker-Finch 2012). The standard AM 1.5 incident illumination spectrum was used throughout all modelling. OPAL 2 is able to model and calculate the photogenerated current as a function of depth for various texturing schemes, anti-reflection coatings (ARC) and incident spectrums. For the purpose of building a baseline IBC solar cell, only one ARC dielectric layer of 85nm SiNx is used in this work. The optical pathlength factor (Z) was modeled using Equation 1. The background bulk lifetime (τ_{bulk}) and effective intrinsic carrier concentration ($n_{i,eff}$) were fixed to 500 µs and $9.65\times10^{9}cm^{-3}$(Mitchell et al. 2012), respectively.

$$Z = 4 + \frac{\ln[n^2+(1-n^2)e^{-4\alpha W}}{\alpha W} \quad \text{(Eq. 1)}$$



(a) (b)

Figure 1 Schematic of *p*-type IBC silicon unit-cell with planar front surface (a) in two-dimensions and (b) in three-dimensions

Table 1 Design parameters for baseline IBC solar cell

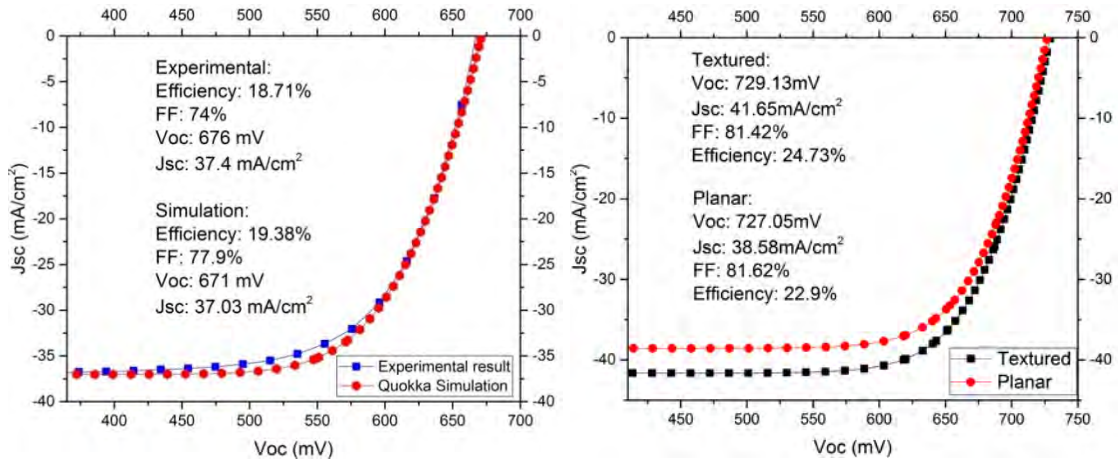
Structure Parameters	*n*-type value	*p*-type value
Emitter half width(x)	62.5 µm	62.5 µm
Emitter half width(y)	60 µm	60 µm
Emitter contact half width	5 µm	5 µm
Contacted emitter J_0	1.16×10^{-12} A/cm^2	1.0×10^{-12} A/cm^2
Passivated emitter J_0	1.895×10^{-14} A/cm^2	5.0×10^{-15} A/cm^2
BSF half width	15 µm	15 µm
BSF contact half width	5 µm	5 µm
Contacted BSF J_0	3.4×10^{-13} A/cm^2	1.0×10^{-13} A/cm^2
Passivated BSF J_0	1.6×10^{-13} A/cm^2	5.0×10^{-14} A/cm^2
Front and rear surface J_0	2.89×10^{-15} A/cm^2	2.89×10^{-15} A/cm^2
Emitter and BSF contact pitch	120 µm	120 µm
External circuit series resistance	0.5 Ωcm^2	0.5 Ωcm^2
External circuit shunt resistance	1x10^5 Ωcm^2	1x10^5 Ωcm^2

At the back surface of the IBC solar cell, a sheet p^+ emitter and localized n^+ back surface field (BSF) was applied with contact opening for the emitter diagonally opposite to the BSF. In between the emitter and back surface field, an undiffused gap was added to prevent any undesired shunting. Finally, the emitter and BSF were covered with a metal contact. Similarly, the *p*-type planar IBC cell was built based on the same cell structure with sheet n^+ emitter and localized p^+ BSF. The basic parameters for both the *n*-type and *p*-type baseline IBC simulation are shown in Table 1.

3. Simulation Results and Discussion

Figure 2(a) presents the *J-V* curve for the simulation and best experimental result (with aperture) for an *n*-type planar IBC solar cell. Simulation results suggest good overall agreement with the experimental cell behaviour. It can be noted that simulation results for cell efficiency only gives a small mismatch and the V_{OC} and J_{SC} values are almost the same compared with the experimental data. A slightly lower *FF* and efficiency are observed in experimental results. Possible reasons for the difference between simulated and measured data are the high injection dependence surface recombination in the gap region or mismatch in voltage at the maximum power point.

The model for the planar *p*-type IBC solar cell had an identical structure to the *n*-type unit cell and achieved an efficiency of 19.03%. Further optimisation was done for a 60µm *p*-type IBC solar cell. The modelled cell in Section 2 yields a high open circuit voltage of 727mV and efficiency of 22.9% by applying the parameters in Table 1. Full *J-V* curves are shown in Figure 2 below.



(a) (b)

Figure 2 (a) Simulated and experimental *J-V* curves for *n*-type IBC solar cell. (b) *J-V* curves of a 60-µm *p*-type IBC cell with and without front surface texturing.

3.1. Light trapping

Increasing absorption within the cell will significantly improve the cell efficiency, primarily by boosting the J_{sc}. The total amount of light absorbed is dependent on the optical path length and the absorption coefficient. Naturally, a thinner substrate results in less silicon substrate to

absorb photons and consequently fewer generated carriers and a reduction in short circuit current density J_{SC}. This problem can be alleviated by applying a light trapping technique on the front surface. Simulations of an IBC solar cell modelled with front surface texturing (random upright pyramids) shows a J_{SC} of 41.65 mA/cm^2, *FF* of 81.42% and V_{OC} of 729 mV, yielding an AM1.5G energy conversion efficiency of 24.73%. The *J-V* curve for this simulation is shown in Figure 2(b). Overall, the application of front surface texturing has improved the *Jsc* by 8% relative compared to the planar front design.

3.2. Bulk minority lifetime and cell thickness

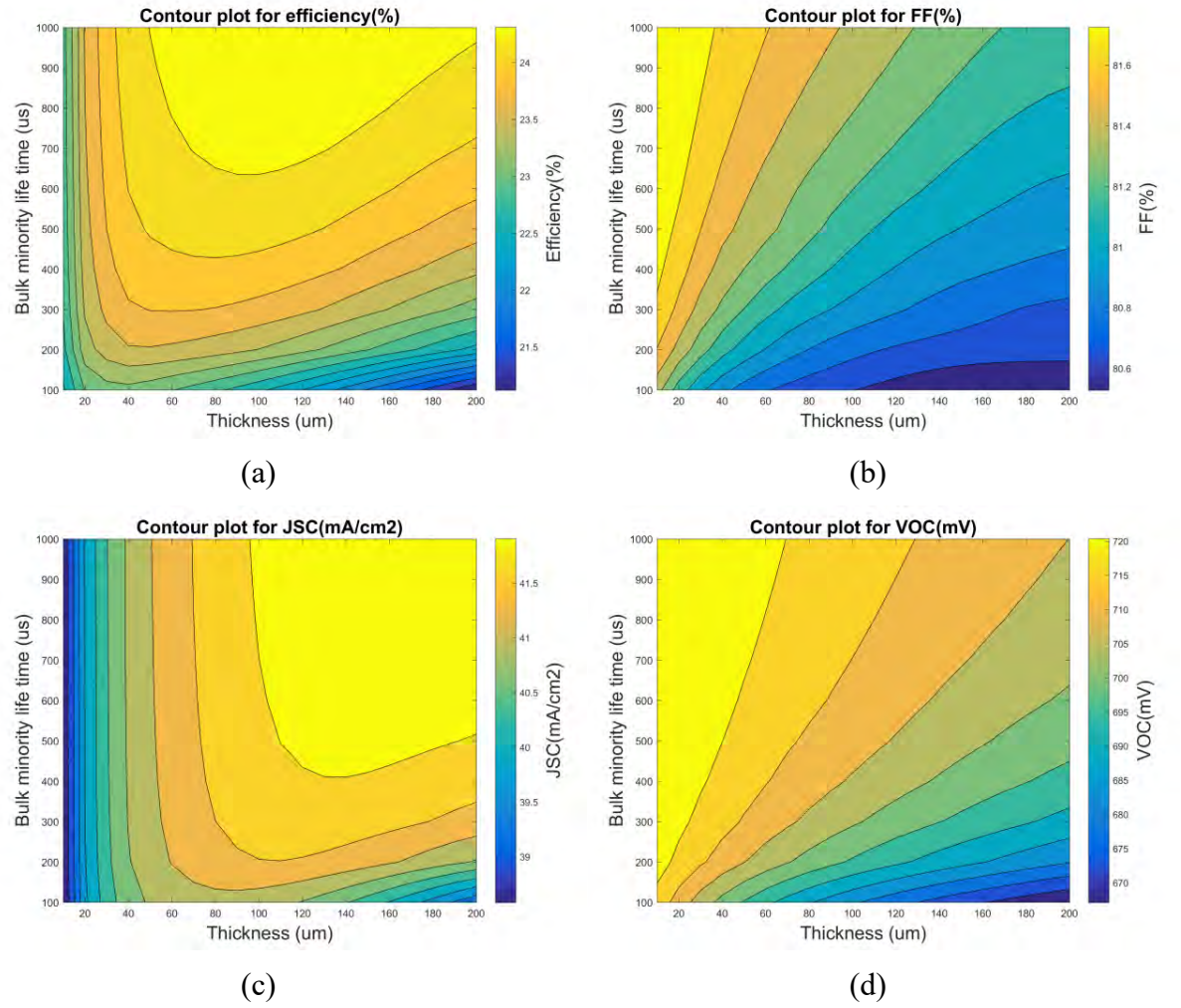


Figure 3 Quokka simulation results for cell efficiency, fill-factor, open circuit voltage and short circuit current for different cell thickness and bulk minority lifetime.

In order to further optimise the *p*-type IBC solar cell behaviour, simulations of varying bulk minority lifetime and substrate thickness were carried out.

Minority carrier lifetime (τ) is a key parameter which indicates the material quality and has a dramatic impact on cell performance. As most of the photogenerated carriers are generated in the vicinity of the front surface, carriers must diffuse through the full thickness of the silicon

in order to be collected at the back of the device. A high minority carrier lifetime is therefore typically required. Poor minority carrier lifetime in the bulk of the solar cell will lead to a significant amount of minority carriers recombining before reaching the contact. However, the effect of the minority carrier lifetime on device performance only holds influence up until a certain level. As shown in Figure 3(a) and 3(c), beyond a certain value, any further improvement on minority carrier lifetime in the bulk does not lead to a significant improvement in cell efficiency and short circuit current.

The cost of the silicon substrates used for device fabrication is critical to the photovoltaics industry. This leads to a natural preference towards thinner wafers, with the current cell substrate thickness for crystalline silicon solar cells at around 60-180 µm (Yu et al. 2012). Thinner wafers can also be achieved by utilising more novel sawing or wafering techniques and therefore potentially further reducing the cost of fabrication.

Referring to Figure 3(b) and (d), with a fixed bulk lifetime, thinner cell thicknesses result in a higher V_{OC} and FF. It can be observed from Equation 2 that the V_{OC} is highly dependent on dark saturation current density, J_0. A thinner substrate will have less recombination in the bulk assuming an identical minority carrier lifetime, thus increases the V_{oc}. In contrast, the J_{SC} decreases significantly as the cell thickness is reduced due to lower optical absorption leading to less carrier generation.

$$V_{OC} = \frac{nkT}{q} ln\left(\frac{J_L}{J_0} + 1\right) \quad \text{(Eq. 2)}$$

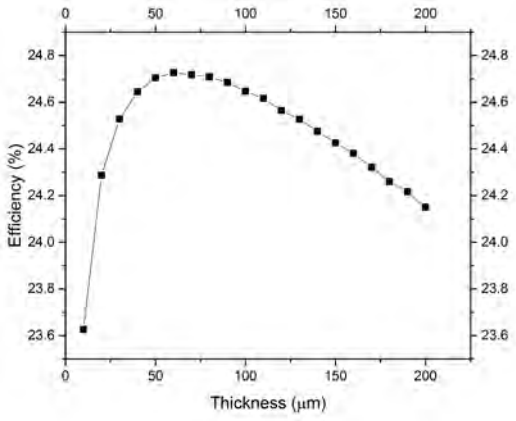


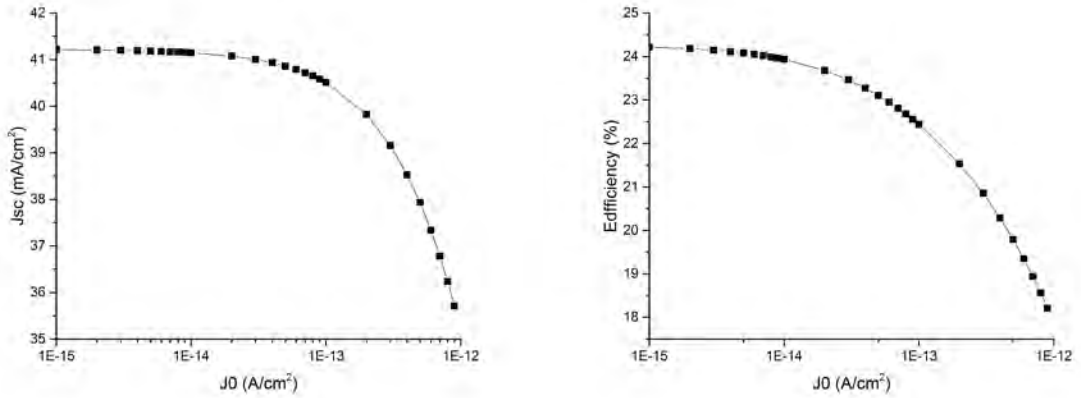
Figure 4 Variation of simulated efficiency for *p*-type IBC solar cell with different cell thicknesses for a fixed bulk minority lifetime and resistivity at 550 µs and 1 Ωcm, respectively.

Figure 4 shows a summary of simulated efficiency with different cell thickness for a fixed bulk minority lifetime and resistivity of 550µs and 1Ωcm respectively. A significant improvement in cell efficiency is initially obtained with increasing thickness, but this quickly plateaus, reaching a peak efficiency of 24.73% for a thickness of 60 µm. The efficiency then starts to decline as the silicon thickness is further increased. As detailed in Section 1, most of the photogenerated carriers are at the front of the device, but some of the carriers are generated further into the bulk. For extremely thin wafers, the device efficiency is limited by the J_{SC}, thus the efficiency initially increases with the thickness. After a certain point (60 µm in this design), the generated carriers become less likely to be collected as larger diffusion

lengths are required. Therefore, a further increase of cell thickness results in a drop in cell efficiency.

3.3. *Front surface J_0*

Front surface passivation quality is critical for IBC solar cells as most of the photogenerated carriers are generated near to this region. It is therefore necessary to critically assess the exact impact of the front surface J_0. Poor front surface passivation causes the photogenerated carriers to recombine with the majority carriers in the bulk rather than diffuse through the wafer, thus poor passivation leads to a reduction in J_{SC} and *Voc*.



(a) **(b)**

Figure 5(a) simulated short circuit current density and (b) efficiency as a function of front surface J_0

Figure 5 plots the cell performance as a function of cell recombination current prefactor, J_0 at the front surface. The simulation was carried out for a fixed thickness, bulk minority lifetime and resistivity of 50µm, 1000µs, and 1 Ωcm respectively. The results confirm that to reach higher energy conversion efficiency and short circuit current density for the *p*-type IBC cell, J_0 values for each contact region must be kept as low as possible. Referring to Figure 5, J_0 values are required to be least keep below $1x10^{-13}$ A/cm^2 if high J_{SC} and cell efficiencies above 40 mA/cm^2 and 22 % respectively are to be obtained.

3.4. *Pitch size*

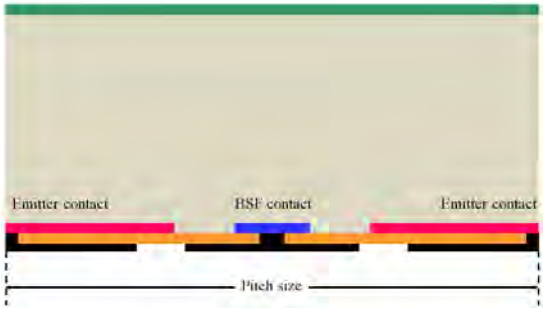


Figure 6 Cross section of *p*-type IBC solar cell with indication of pitch size

Pitch size represents the distance between any adjacent emitter (or BSF) contact. Figure 6 demonstrates a schematic showing definition of pitch size in this context. Contact formation can be carried out using simple screen printing techniques for larger pitch sizes whilst more

complex lithography processes are required when pitch size is reduced as this requires a finer pattern on the surface. Figure 7 shows the modelled cell performance as a function of pitch size. The contact size for both emitter and BSF are fixed and the pitch distance was varied from 160µm to 2000µm. The cell efficiency starts to drop significantly when the pitch size is larger than 400 µm in this design because of the series resistance effect. A larger pitch reduces the carrier collection probability in the bulk of the device. Carriers generated near the front of the device move in vertical and lateral directions. A larger pitch size naturally increases the lateral distance for the generated carriers to be collected at the back of the device, therefore increasing the likelihood of carriers to recombine in the bulk (Kluska et al. 2010). A smaller pitch size leads to an increased open circuit voltage due to lower saturation current density J_0 of the device. A higher Fill factor (*FF*) can also be achieved by reducing the pitch size as lateral resistance losses are reduced. However, the short circuit current is reduced with increasing pitch size as the emitter coverage is reduced.

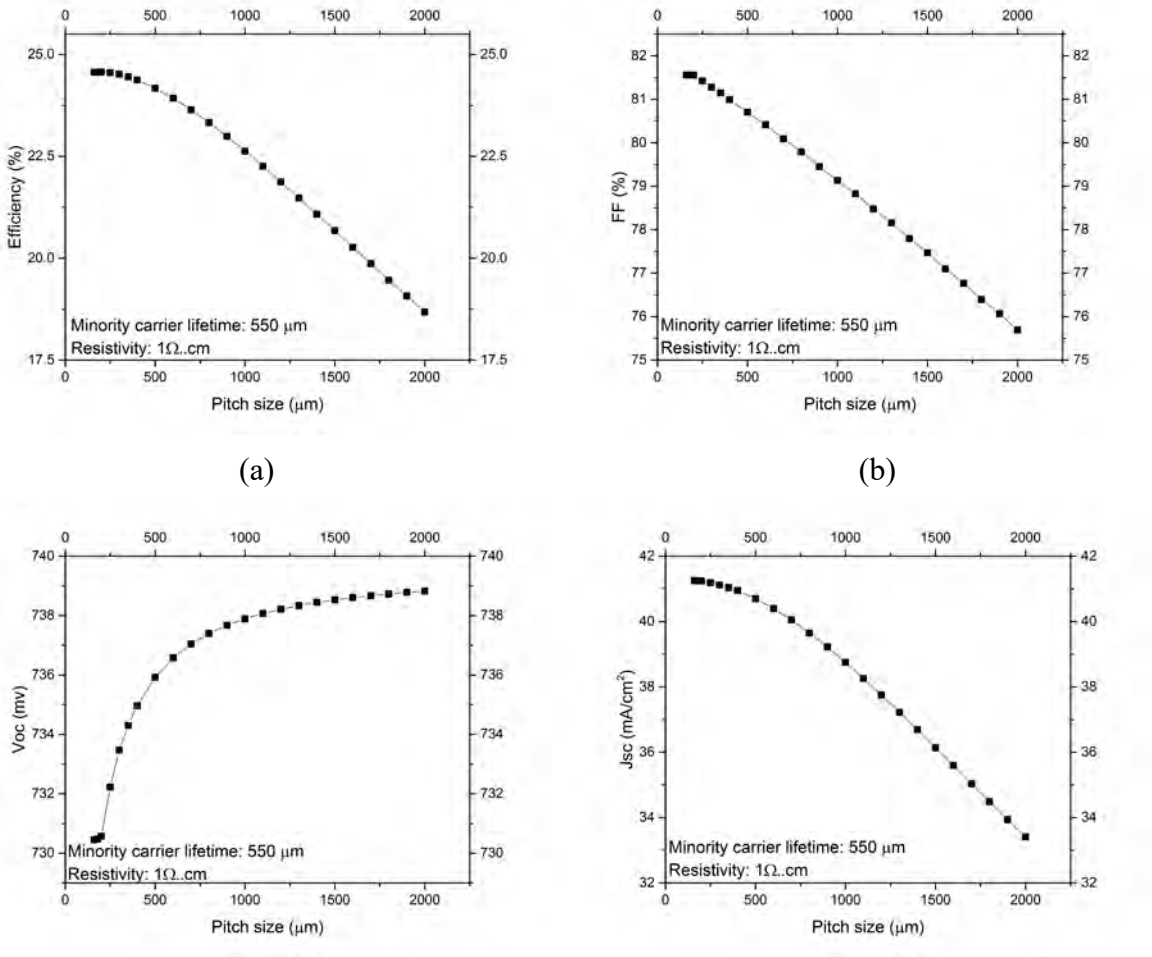
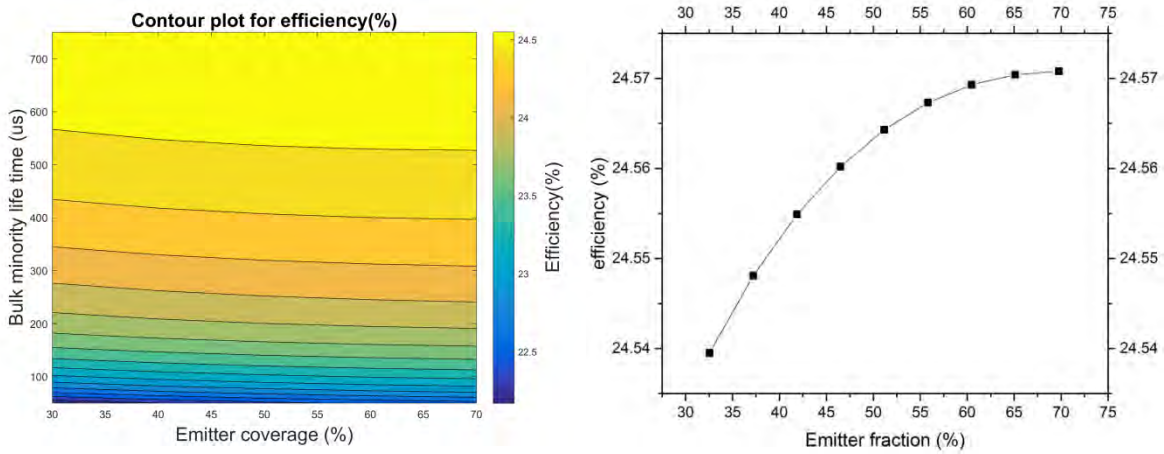


Figure 7 Quokka simulation results for cell efficiency, Fill-factor, open circuit voltage and short circuit current for different pitch size.

3.5. Emitter fraction

Photogenerated electron-hole pairs are separated at the emitter region. IBC solar cell performance depends on the emitter coverage over the base and its effect is shown in Figure 8. In this case the pitch size and bulk resistivity were fixed at 215 µm and 1 Ωcm respectively. Emitter fraction is increased from 30-70% and the minority lifetime in the bulk varied between 30-750µs. Figure 8(a) shows that the emitter fraction has a negligible effect on cell efficiency regardless of the minority lifetime in the bulk, which implies cell designs are more tolerant against fabrication error in the size of the emitter. A more clear relationship between emitter fraction and efficiency at fixed bulk minority lifetime of 550µs is shown in Figure 8(b)



(a) (b)

Figure 8 modelled cell efficiency with (a) combined bulk minority lifetime and emitter fractions (b) only impact on different emitter fractions at fixed lifetime of 550µs

4. Conclusion

Three-dimensional Quokka simulations were carried out in order to validate against *n*-type experimental samples. Further simulation is performed to design and investigate for a high-performance *p*-type interdigitated back contact silicon solar cell. The influence of different solar cell parameters over the *p*-type IBC cell performance was studied and a detailed analysis based on the impact of light trapping and passivation on the front surface, variation of cell geometry on the back contact, and base material quality was carried out. The results confirm that short circuit current density is highly dependent on the front surface passivation and light trapping quality as well as the emitter fraction on the back surface. Fill factor increases as the pitch and emitter fraction decreases due to the reduction of the lateral resistance losses. With the investigation of cell parameters, optimized cell energy conversion efficiency can be achieved at 24.73 % for a *p*-type IBC solar cell with a 60µm cell thickness and 550µs in minority lifetime in the bulk.

References

Fell, A. et al., 2014. 3-D Simulation of Interdigitated-Back-Contact Silicon Solar Cells With Quokka Including Perimeter Losses. *IEEE Journal of Photovoltaics*, 4(4), pp.1040–1045.

Fell, A., 2013. A Free and Fast Three-Dimensional/Two-Dimensional Solar Cell Simulator Featuring Conductive Boundary and Quasi-Neutrality Approximations. *IEEE Transactions on Electron Devices*, 60(2), pp.733–738.

Kluska, S. et al., 2010. Modeling and optimization study of industrial n-type high-efficiency back-contact back-junction silicon solar cells. *Solar Energy Materials*.

Lammert, M. & Schwartz, R., 1977. The interdigitated back contact solar cell: a silicon solar cell for use in concentrated sunlight. *IEEE Transactions on Electron*.

Lu, M. et al., 2007. Interdigitated back contact silicon heterojunction solar cell and the effect of front surface passivation. *Applied Physics Letters*.

Lu, M. et al., 2009. Optimization of interdigitated back contact silicon heterojunction solar cells by two-dimensional numerical simulation. In *2009 34th IEEE Photovoltaic Specialists Conference (PVSC)*. IEEE, pp. 001475–001480.

Masuko, K., Shigematsu, M. & Hashiguchi, T., 2014. Achievement of more than 25% conversion efficiency with crystalline silicon heterojunction solar cell. *IEEE Journal of*.

McIntosh, K. & Baker-Finch, S., 2012. OPAL 2: Rapid optical simulation of silicon solar cells. *Specialists Conference (PVSC) …*.

Mitchell, B., Greulich, J. & Trupke, T., 2012. Quantifying the effect of minority carrier diffusion and free carrier absorption on photoluminescence bulk lifetime imaging of silicon bricks.

Smith, D.D. et al., 2014. Toward the Practical Limits of Silicon Solar Cells. *IEEE Journal of Photovoltaics*, 4(6), pp.1465–1469.

Walter, D. & Schmidt, J., 2016. Impact of hydrogen on the permanent deactivation of the boron-oxygen-related recombination center in crystalline silicon. *Solar Energy Materials and Solar Cells*.

Yu, X. et al., 2012. Thin Czochralski silicon solar cells based on diamond wire sawing technology. *Solar Energy Materials and Solar Cells*.

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