# A Step by Step Optimisation of c-Si Bottom Cell in Perovskite/c-Si Tandem Devices

YiLiang Wu[1], Andreas Fell[2] and Klaus J. Weber[1]

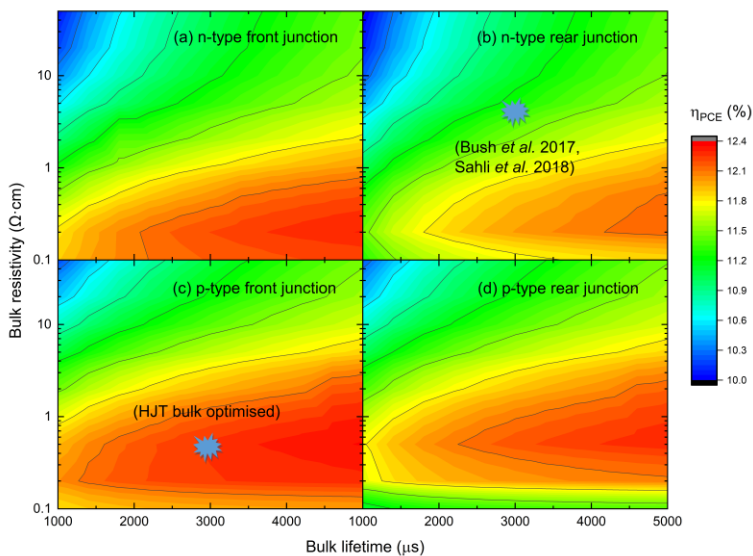*[1]Research School of Engineering, Australian National University, Canberra, Australia*
*[2]Fraunhofer Institute of Solar Energy Systems, Freiburg, Germany*
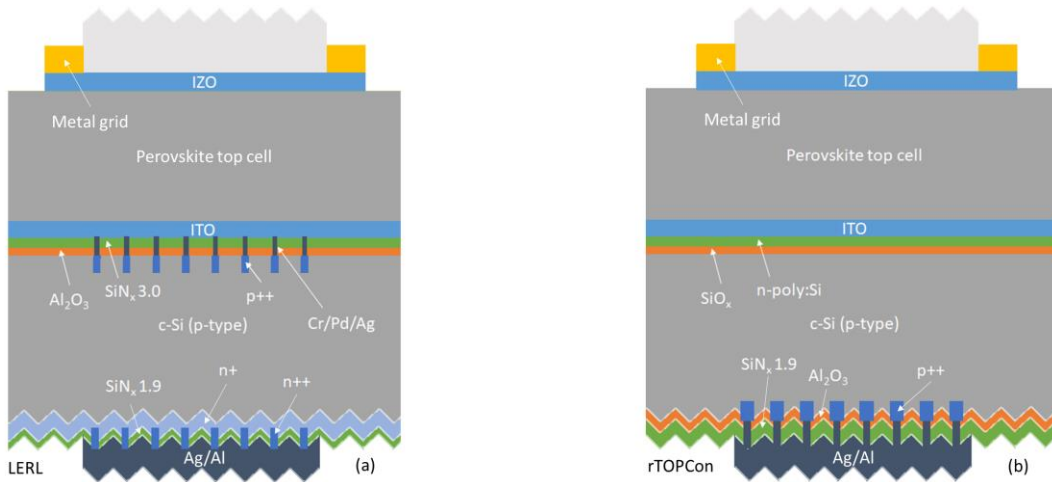*E-mail: yiliang.wu@anu.edu.au*

Perovskite/c-Si tandem devices are of great interest as potential candidates for next-generation photovoltaic devices. Such devices could combine a higher efficiency than c-Si with an acceptably low production cost to enable further reductions in PV System costs. To date, little attention has been paid to the optimisation of the c-Si bottom cell in these devices. However, for the highest possible efficiency, such an optimisation is necessary.

Here, we use numerical modelling to rigorously analyse the impact of both material properties (doping type and concentration) and device architecture on the efficiency of the c-Si cell. We focus on silicon cells with a planar front and textured rear surface. While excellent results have recently been demonstrated with front both surfaces textured cells, our simulation results show rear textured cells can achieve similar current generation. Importantly, the use of a textured front surface severely restricts the range of processes available for the deposition of the perovskite cell constituent layers.
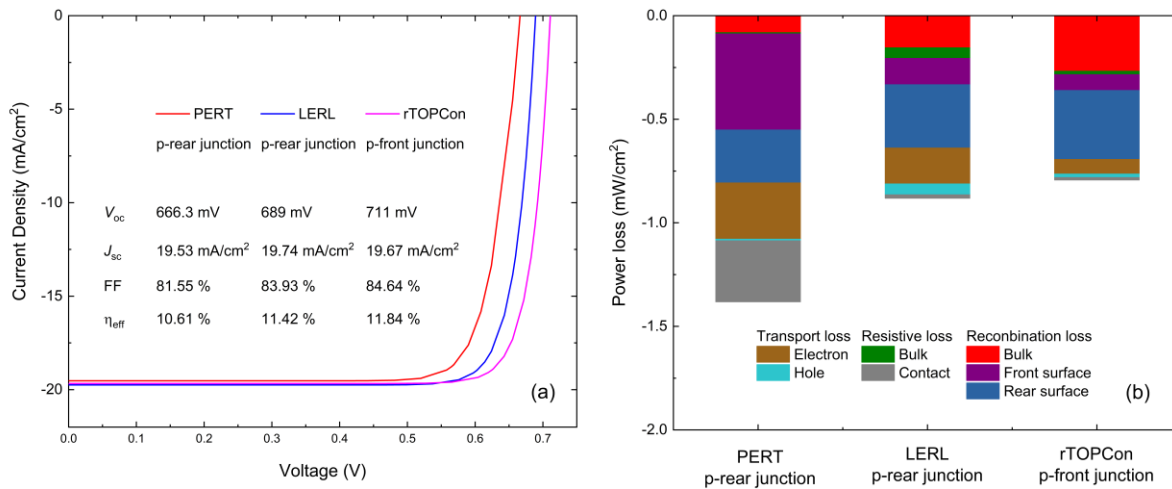
We show that the use of low resistivity p-type wafers can result in higher efficiencies than the currently favoured n-type, moderate resistivity wafers, for both homojunction and heterojunction bottom c-Si devices. Two new device structures - Localized Emitter Rear Localized diffused (LERL) and reversed Tunneling Oxide Passivating Contact (rTOPCon) are proposed in order to further simplify cell fabrication and improve the device efficiency. We show that these structures are capable of the same high efficiencies as heterojunction cells while offering substantially greater temperature tolerance for the deposition of the perovskite top cell. The implementation of such optimised c-Si bottom cells will be crucial to the achievement of 30% efficient tandem devices.



**Figure 1.** The simulated efficiency of the HJT c-Si bottom cell in relation to the bulk resistivity and lifetime with (a) n-type wafer with front junction structure, (b) n-type wafer with rear junction structure, (c) p-type wafer with front junction structure, and (d) p-type wafer with rear junction structure

**Figure 2.** Device schematic drawing for monolithic perovskite/c-Si tandem with the bottom cell structure using (a) LERL, (b) rTOPCon.



**Figure 3.** (a) Simulated *JV* curve of the c-Si bottom cell with different design structures. (b) Power losses using a free energy loss analysis (FELA) in different design structures at the maximum power point, for ease of reading, optical losses are not presented.