Australian National University

A Step by Step Optimization of the c-Si Bottom Cell in Monolithic Perovskite/c-Si Tandem Devices

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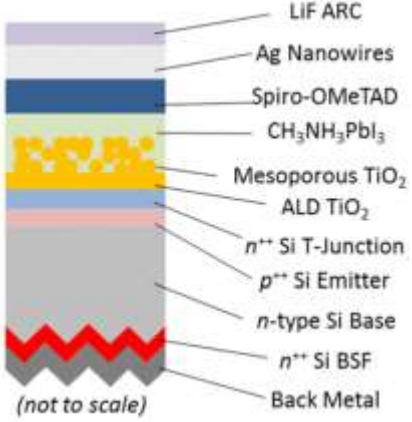
The rapid evolution



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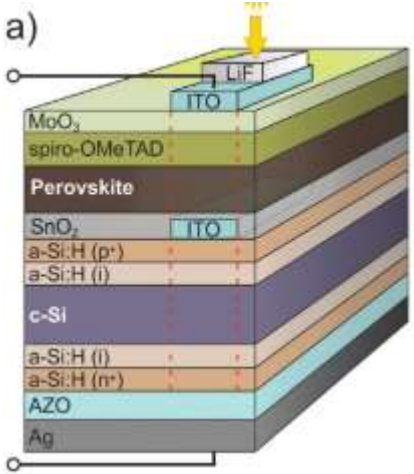

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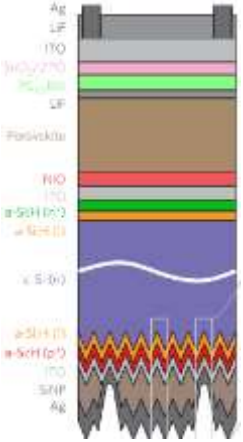
Albrecht, S., et al. *Energy Environ. Sci*. 9 (2016)



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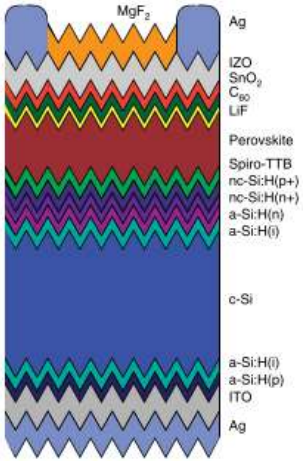


25.2%

Sahli, F., et al. *Nat. Mat.* (2018)

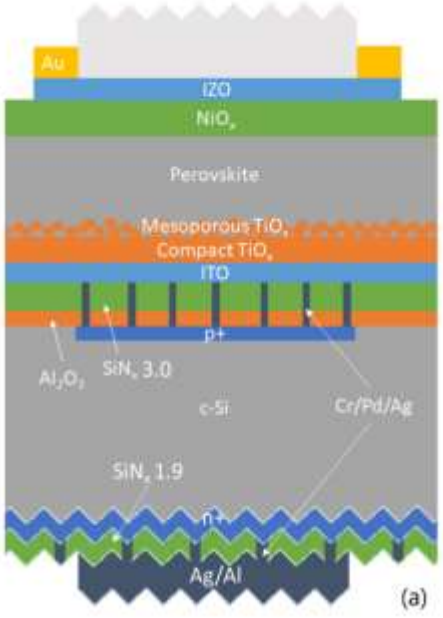
27.3%

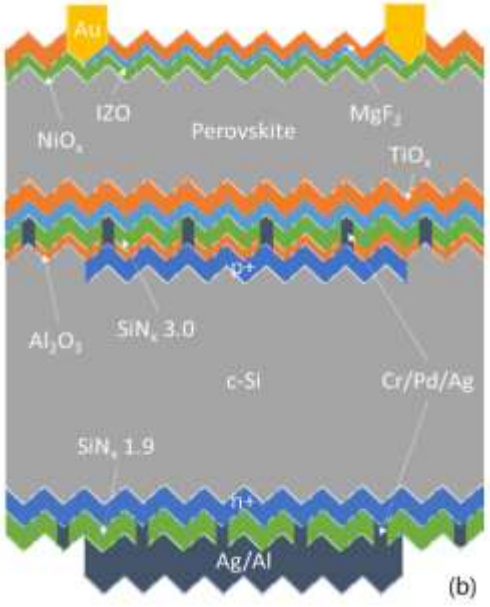
Oxford PV, *News release.* (2018)

Mailoa, J., et al. *Appl. Phys. Lett.* 106 (2016)

Bush, K., et al. *Nat. Energy* 2 (2017)

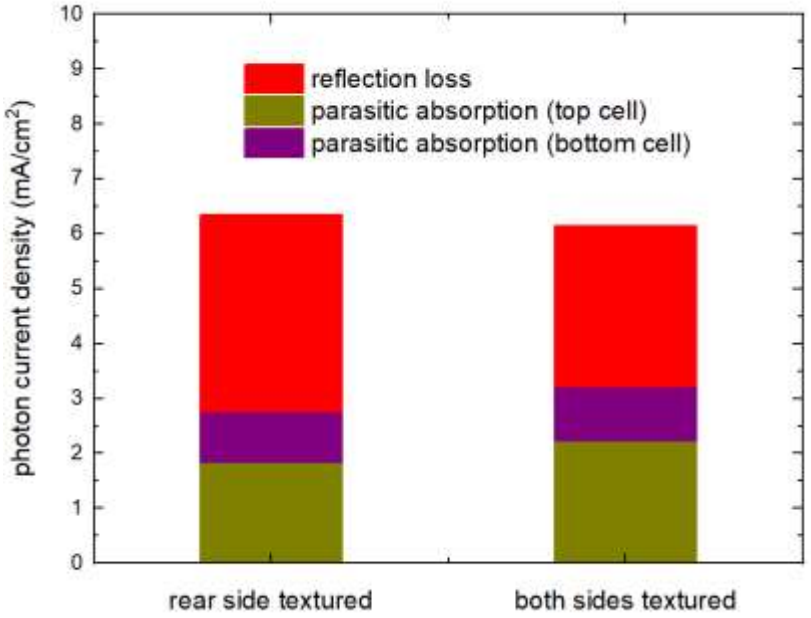
Rear or both sides texturing?





*not to scale

Rear or both sides texturing?



		rear side textured		both sides textured	
		thickness	loss (mA/cm²)	thickness	loss (mA/cm²)
reflection loss	reflected		0.063		1.774
	escaped		3.518		1.166
parasitic absorption loss top cell	silicone foil	400 µm	0.265	n/a	n/a
	Au (front finger)	100 nm	0.336	100 nm	0.262
	MgF_2	n/a	n/a	100 nm	0.627
	IZO	40 nm	0.609	40 nm	0.698
	NiO_x	50 nm	0.624	50 nm	0.653
	perovskite	**310 nm**	**19.98**	**310 nm**	**20.08**
	ms-TiO_2	60 nm	0.0001	n/a	n/a
	cp-TiO_2	50 nm	0.001	50 nm	0.001
parasitic absorption loss bottom cell	ITO	20 nm	0.241	20 nm	0.340
	SiN_x/Al_2O_3	50/10 nm	0.144	50/10 nm	0.140
	c-Si	**280 µm**	**19.99**	**290 µm**	**20.08**
	SiN_x	70 nm	0.006	70 nm	0.004
	Ag/Al	100/700 nm	0.540	100/700 nm	0.486

Rear or both sides texturing?

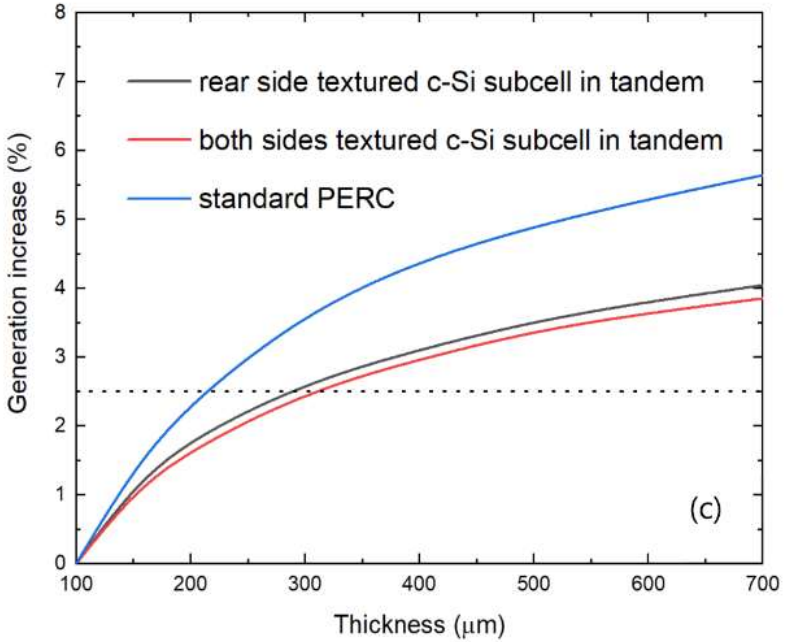
Both sides

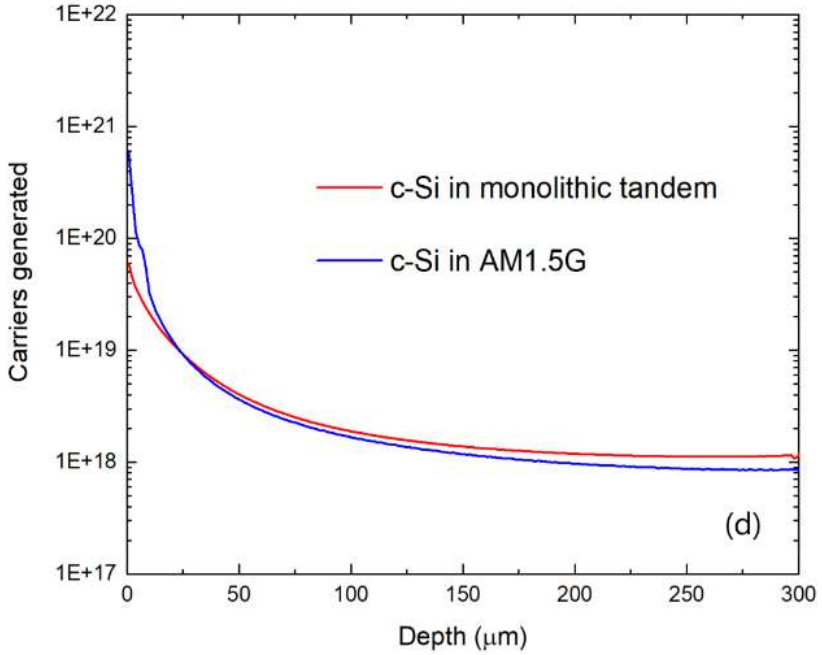
Deposition of perovskite cell on textured surface can be problematic

Rear side only

- Refractive index of TCO and charge transport must be carefully managed to reduce the escaped light
- An anti-reflection foil must be implemented, but can be replaced by structured glass for module application

What has changed?



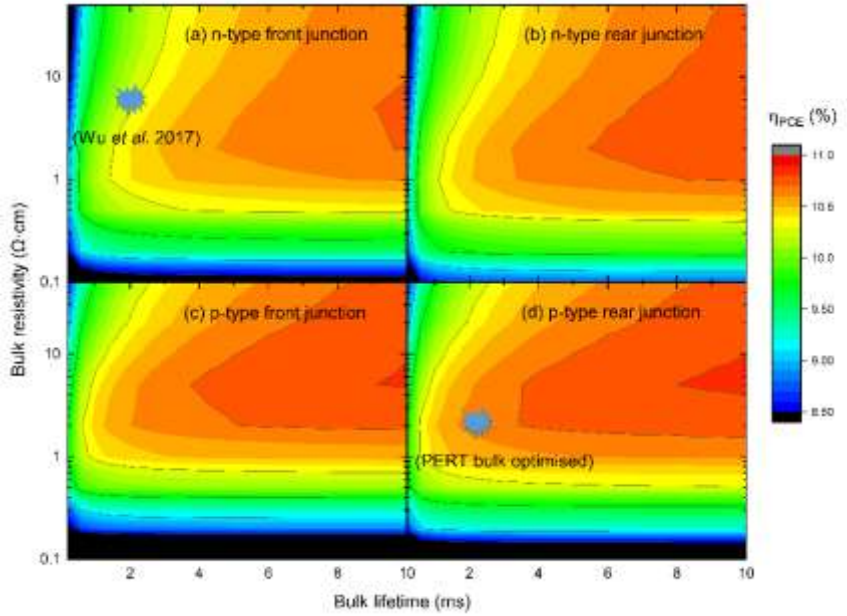


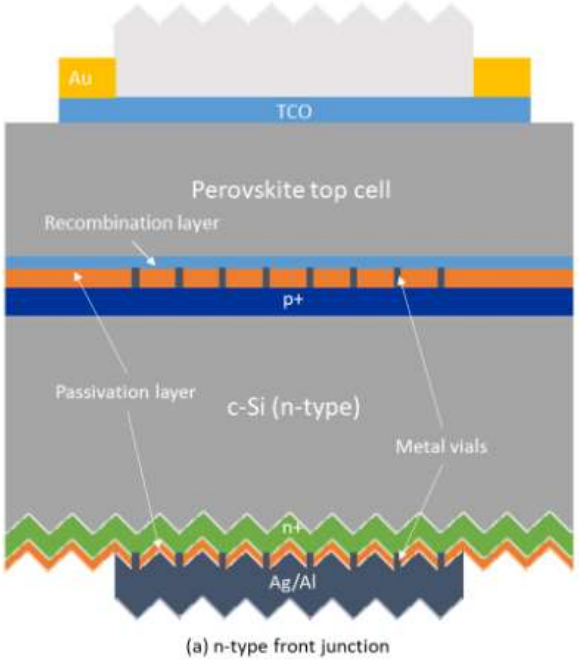
What has changed?

- Increased wafer thickness for tandem application
- Significantly more uniform generation profile

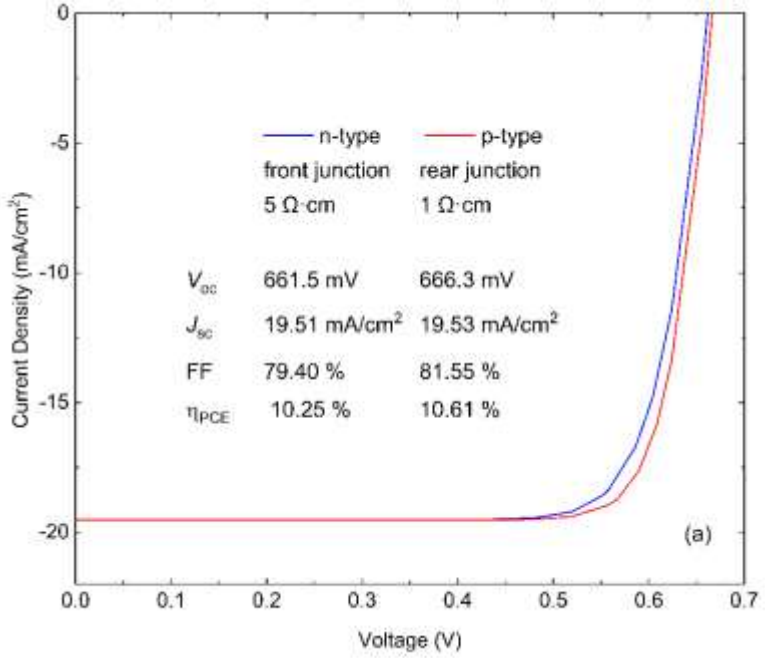
Simulated result by  Quokka3

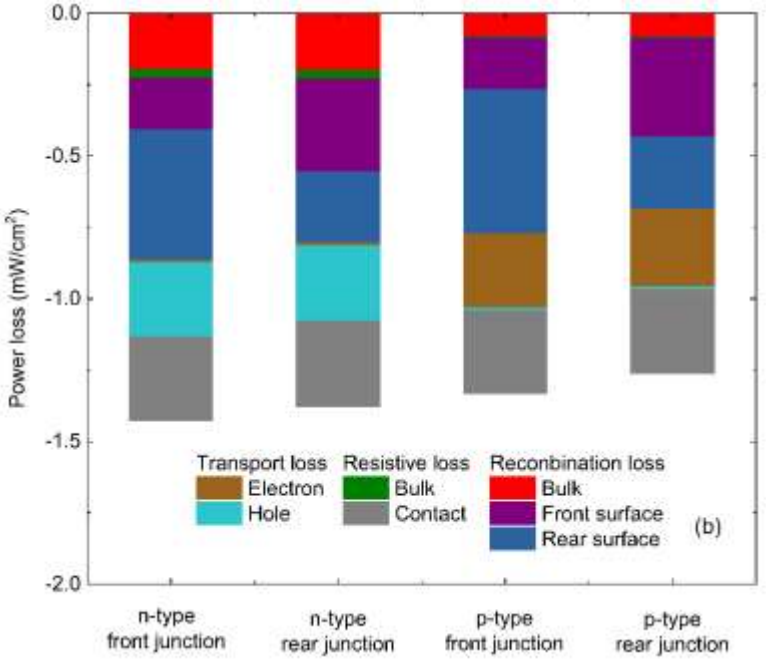
c-Si bulk optimization (PERT)



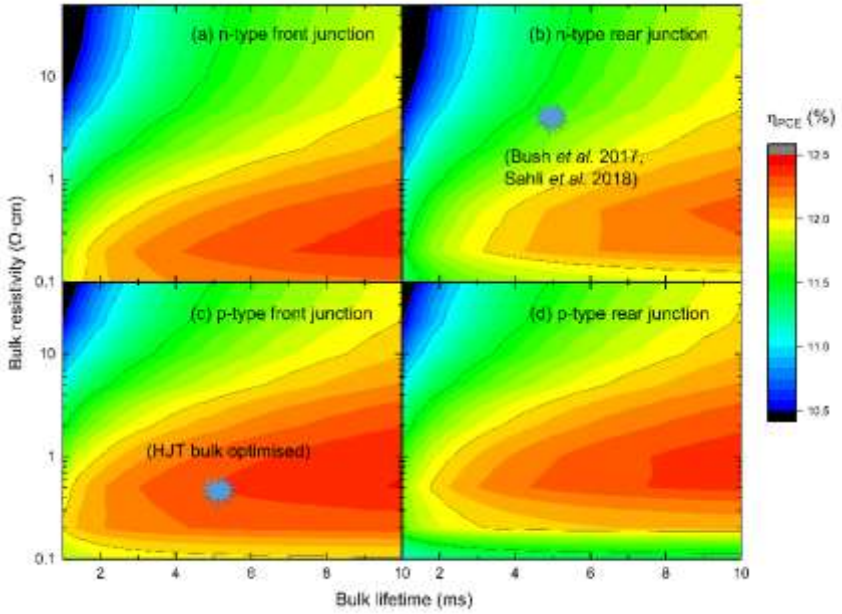


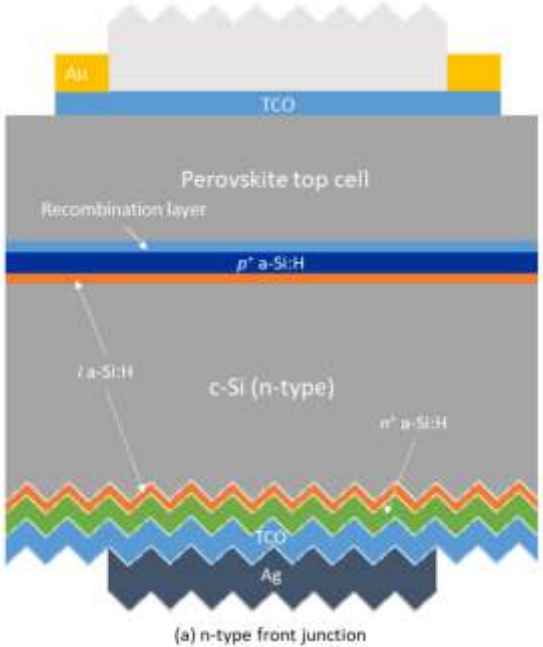
c-Si bulk optimization (PERT)





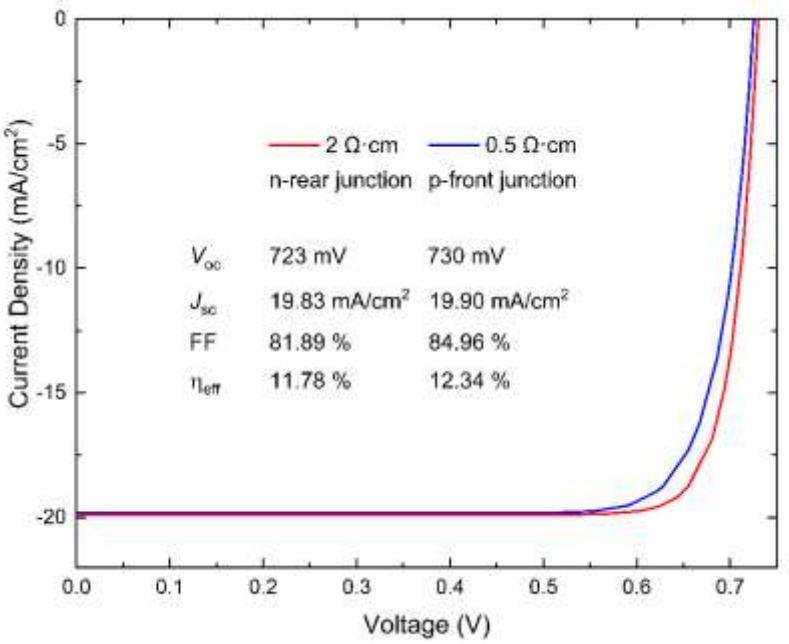
c-Si bulk optimization (HJT)





(a) n-type front junction

c-Si bulk optimization (HJT)



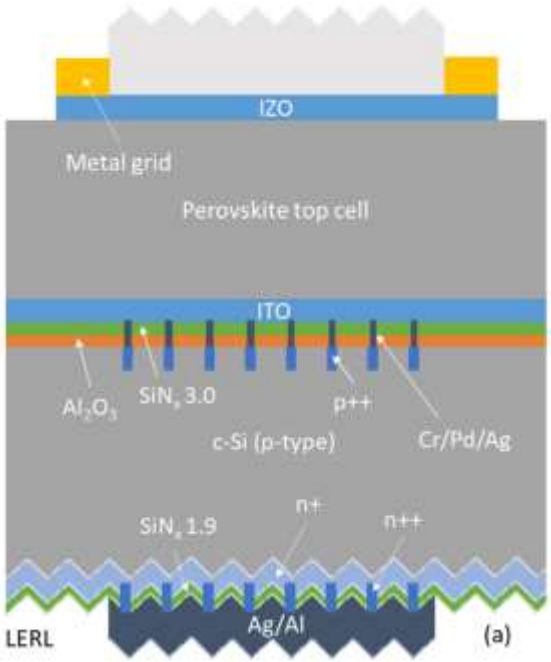
Parameters	n-front junction		n-rear junction		p-front junction		p-rear junction	
$\tau_{bulk\ fixed}$ (ms)	1 ~ 10							
R_{bulk} (Ω·cm)	0.1 ~ 50							
R_{sheet} (Ω/□)	120							
$\rho_{contact}$ (mΩ·cm²)	5							
Side	Front	Rear	Front	Rear	Front	Rear	Front	Rear
$J_{0\text{-contacted}}$ (fA/cm²)	2	3	2	3	2	3	2	3

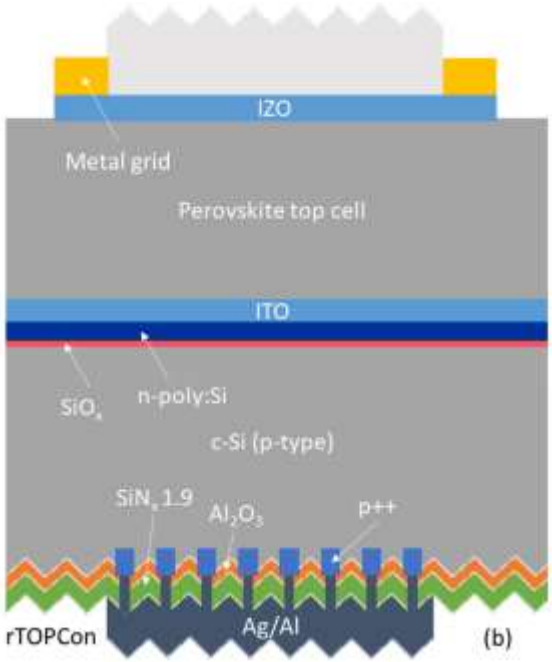
c-Si bulk optimization

- p-type wafers are more suitable
- relatively low resistivity
- front or rear junction is not very important

LERL and rTOPCon

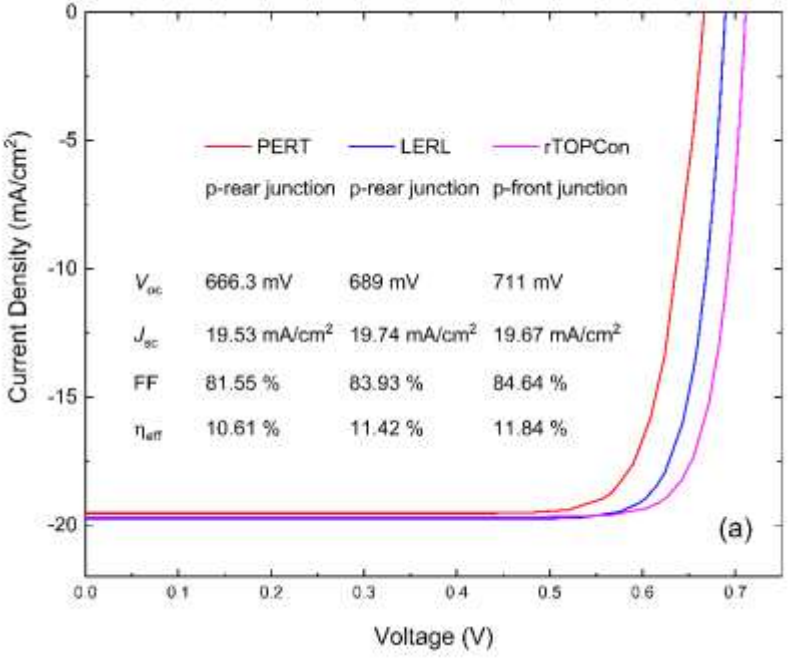
n-i-p

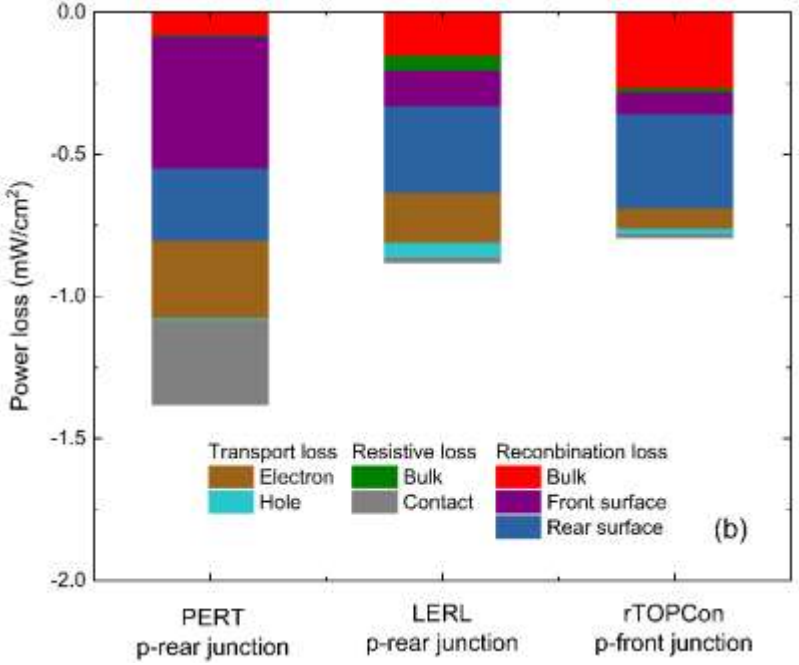




p-i-n

LERL and rTOPCon





Conclusions

- Rear and double sided texturing show similar generation
- p-type wafers are found to be a more suitable candidate for fabricating high efficiency monolithic tandem device
- LERL and rTOPCon are proposed for better bottom cell structures

Acknowledgements

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