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Fabrication of the monolithic perovskite/c-Si tandem solar cells using industrially relevant approach

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A 4-cm^2 large area monolithic perovskite/c-Si tandem solar cell is demonstrated in this work. The top solution processed perovskite device is based on a c-Si bottom cell fabricated on an industrial production line. The bottom device is double side passivated and can be high temperature processed (~500 ˚C) to tolerate any processing requirement from the top perovskite cell. The front surface of the c-Si wafer is non-polished and instead features the surface roughness typical of commercial Si wafers produced by wire sawing. A 21.16% efficiency (certified) with negligible hysteresis is achieved. This result shows the potential of fabricating large area monolithic tandem devices using commercially available c-Si bottom cell with cheap solution process methods.

Fig. 1a shows the structure of the monolithic tandem cell. Additional to our previous result,[1] the c-Si bottom cell was redesigned to facilitate the use of industrial fabrication processes. Firstly, we used n-type polysilicon as the front side passivating contact to achieve state-of-art front surface passivation. As we discussed in our previous work,[2] the reversed TOPCon structure not only provides high efficiency, it can also tolerate over 500 °C post-processing, which is important for the deposition of some stable inorganic charge transport layers, such as TiO_2. The rear side of the device is textured and capped by an AlO_x/SiN_x stack to better harvesting the infrared light. The rear contact is opened by standard industrial laser processing and finished with full area aluminium screen printing. For the recombination layer, a thin layer (2 nm) of ITO was sputtered on top of the n:poly-Si. The interlayer free approach was also attempted but sputtered NiO_x cannot form an ohmic contact with n:poly-Si, which was consistent with the report using solution processed NiO_x on c-Si wafer.[3]

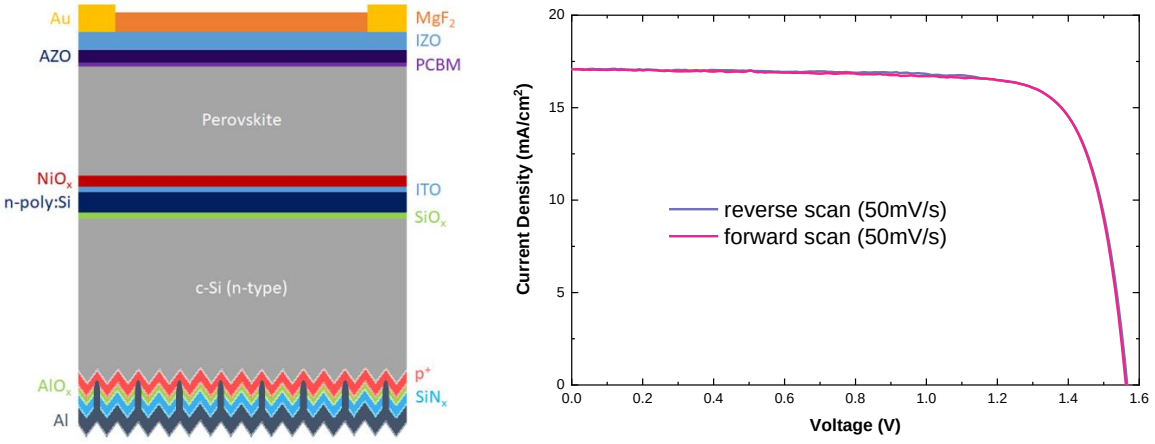

Figure 1. (a) The schematic drawing of the perovskite/c-Si monolithic tandem solar cell (not to scale), (b) In house measured IV curve of the 4 cm^2 monolithic tandem device.

The rough surface morphology of the wafer was found to be the most challenging part of this work. As illustrated in Fig 2, the surface is rough due to wire saw damages, which the subsequent wafer etching

step reduces only to a limited extent. The RMS around 2 µm which is significantly larger than the thickness of the perovskite film (~400-600 nm). This leads to an increased risk of shunting due to pinholes in the perovskite film. To obtain a perovskite top cell with an acceptable level of shunting, firstly we start with a layer of dense and compact NiO_x hole transport film deposited by RF magnetron sputtering. Secondly, while we still use solution processing to deposit the perovskite film, the vacuum flash method was adapted. In this work, the perovskite precursor uses pure DMF solution as introduced by Din et al.[4] The resulting fast and uniform nucleation allows forming a large area, compact and pin-hole free perovskite film on top of the unpolished surface. PCBM was used to extract electrons on the top of the device, capped by an AZO buffer layer and an IZO transparent conductive layer through a sputtering process. A gold grid is used for the front contact, and the cell is finished with a layer of MgF_2 to minimize the reflection loss.

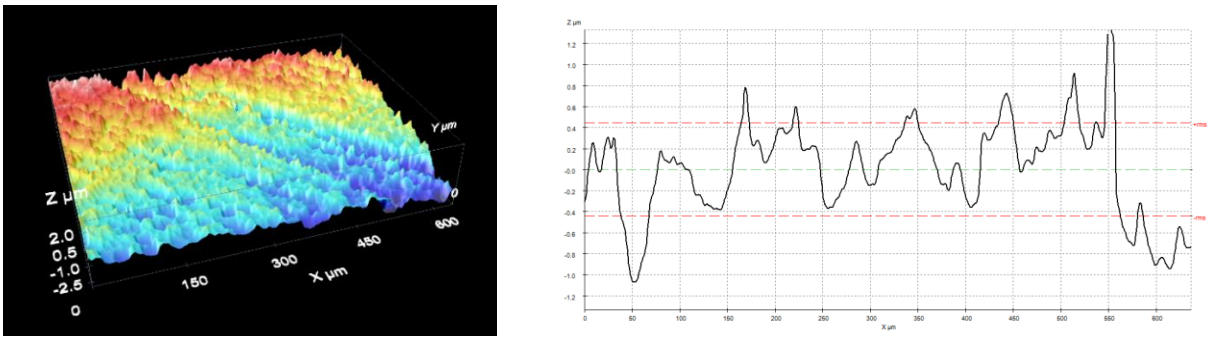

Figure 2. Surface morphology of the front side of the c-Si wafer used for monolithic tandem fabrication in this work, (a) 3D plot, (b) cross-section plot (x and y-axis are not in the same scale)

The device demonstrated here offered a great hope to commercialize the perovskite/c-Si monolithic tandem device in the future without using expansive polished silicon wafer and vacuum processes for perovskite layer deposition.

References

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