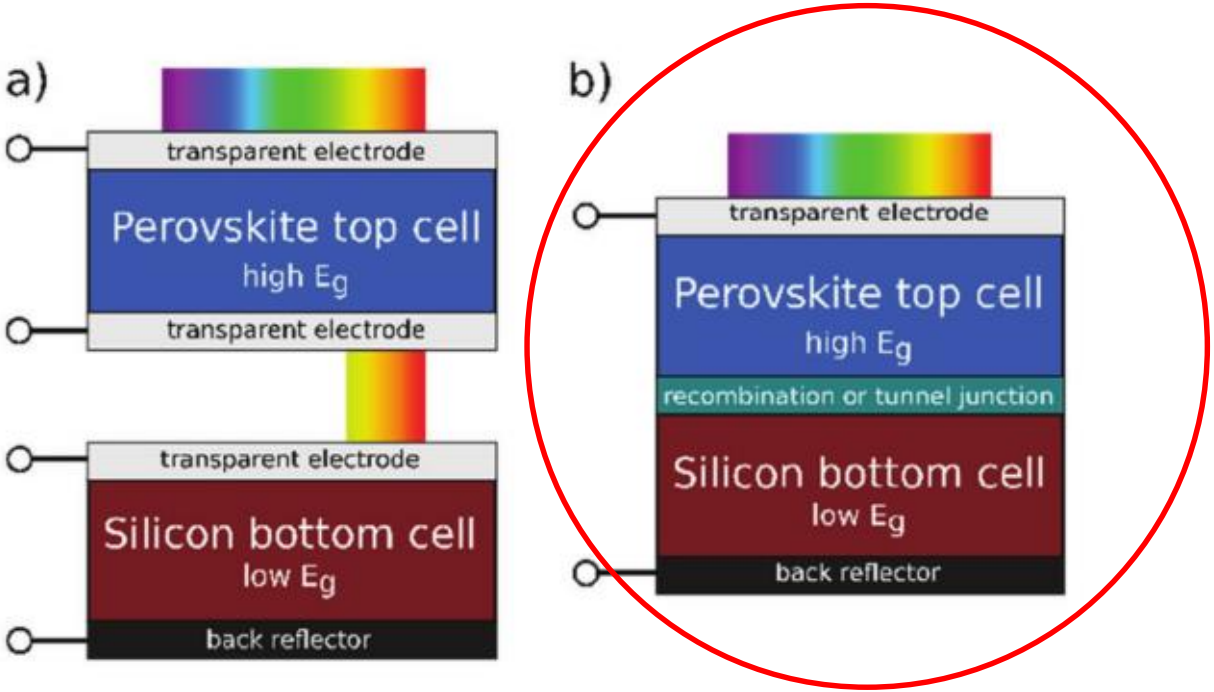
Australian National University

Monolithic perovskite/c-Si tandem solar cell using industrial approaches

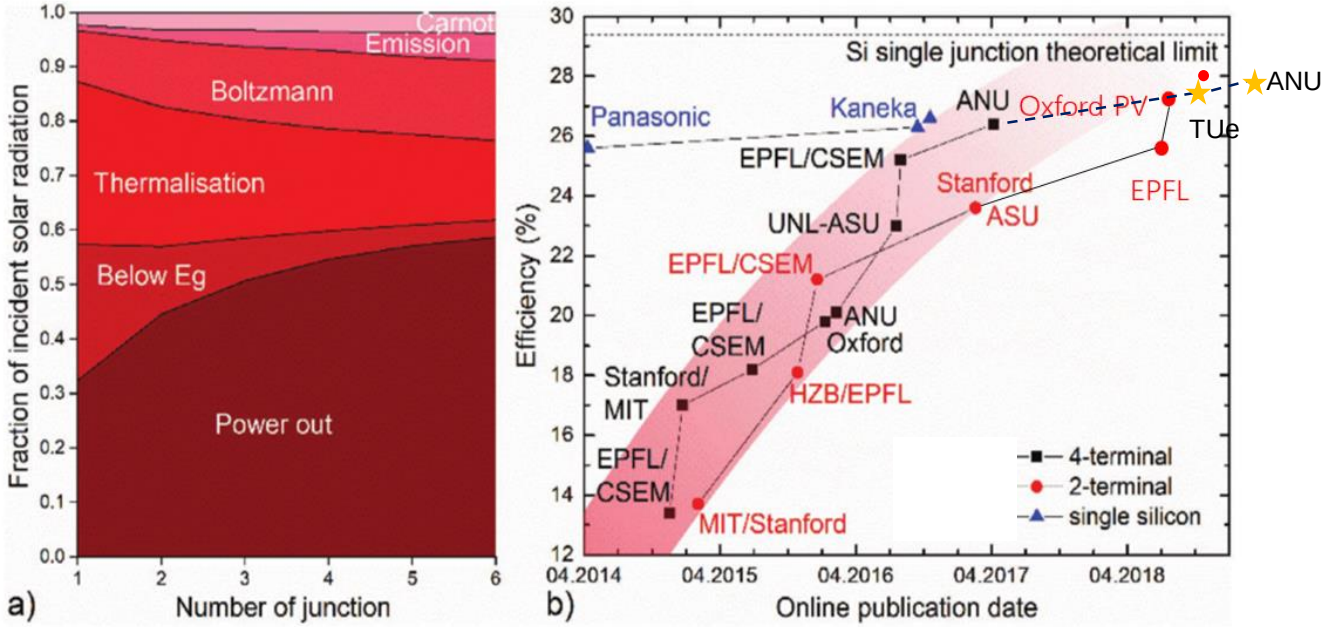
Yiliang Wu

APSRC-2019

Tandem architectures

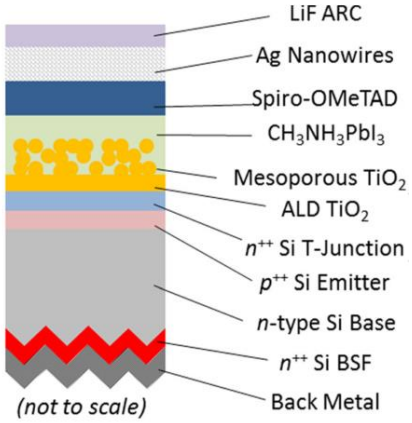


Why tandem?

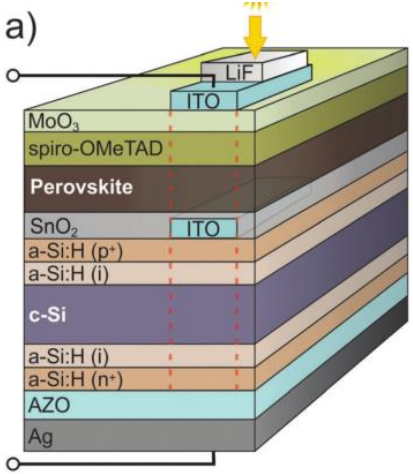


Werner, Jérémie, et al. *Adv. Mat. Interfaces* 5.1 (2018): 1700731

The rapid evolution

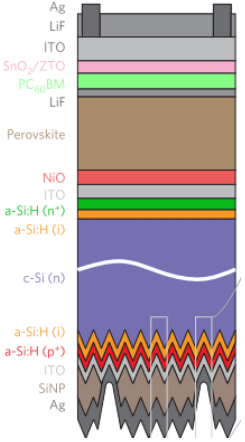


13.7%

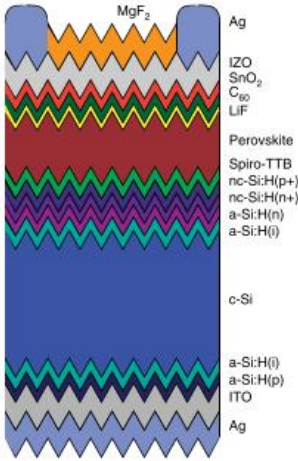


18.1%

Albrecht, S., et al. *Energy Environ. Sci*. 9 (2016)



23.6%



25.2%

Sahli, F., et al. *Nat. Mat.* (2018)

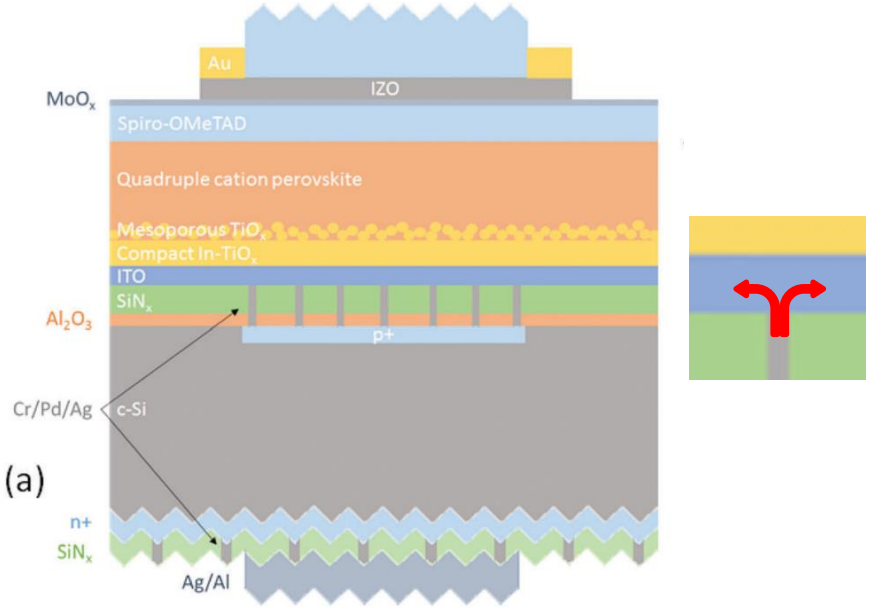
28%

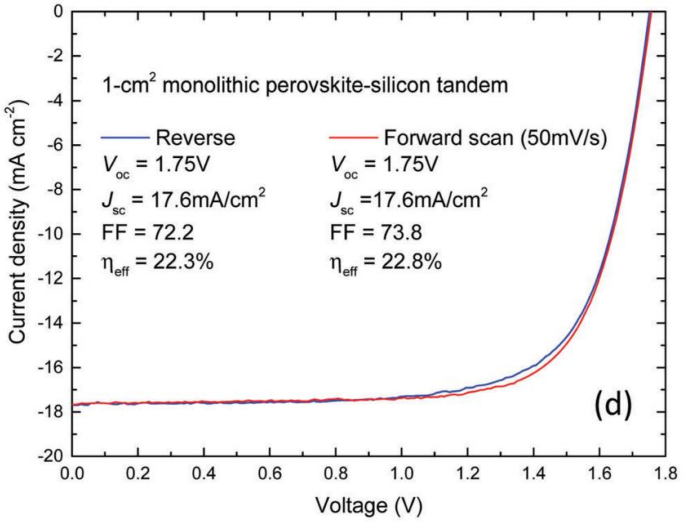
Oxford PV, *News release.* (2018)

Mailoa, J., et al. *Appl. Phys. Lett.* 106 (2016)

Bush, K., et al. *Nat. Energy* 2 (2017)

Monolithic tandem with homojunction technology

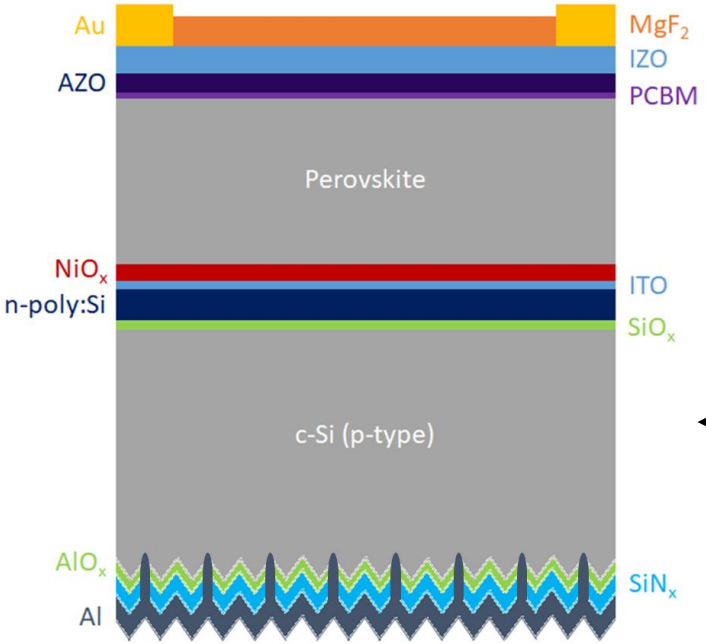




Objectives

- Replace the slow and expensive evaporation process for C_{60}, LiF, perovskite with solution process.
- Use the industrial standard diamond wire cut wafer to replace chemical or mechanically polished wafer.
- Design a bottom c-Si cell can be fabricated on the existing production line.
- Fabricate a 4-cm^2 large area tandem device to validate the design.

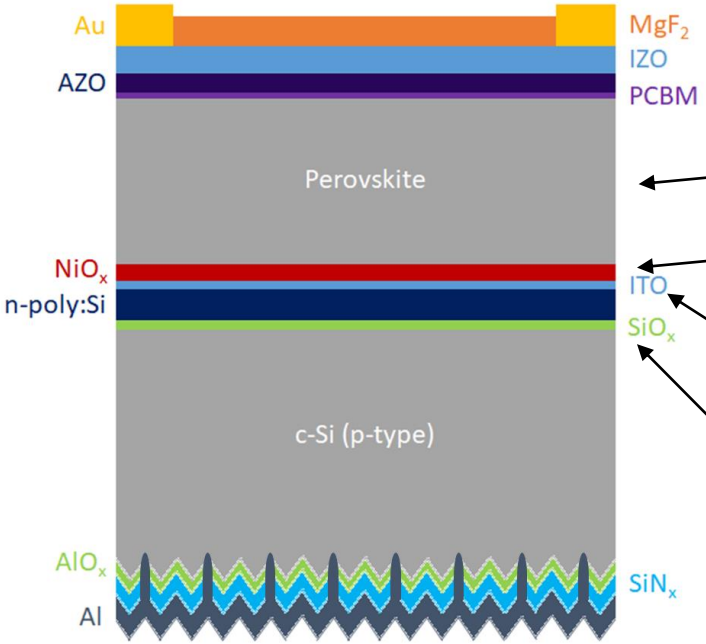
Key features (1)



Solution process top cell (perovskite, PCBM, AZO-np)

1. Cz mono-Si wafer cut by diamond wire without polishing steps
2. Bottom cell fabricated on the industrial production line
3. Reversed TOPCon structure for better efficiency, stability and up to 500 °C temperature tolerance

Key features (2)



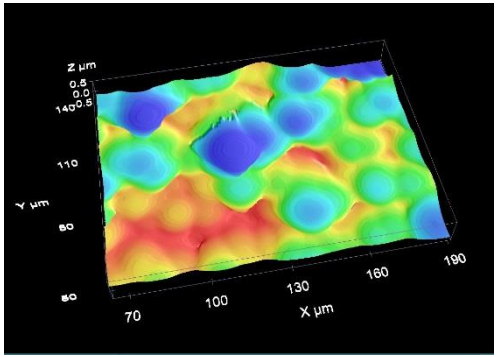
Uniform perovskite layer processed with vacuum flash

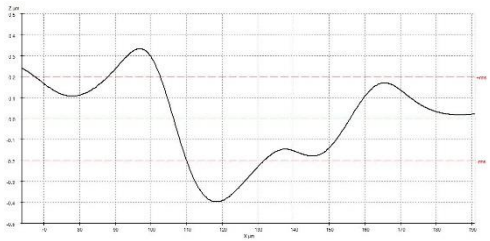
Sputtered NiO_x offer a compact and efficient hole transport layer

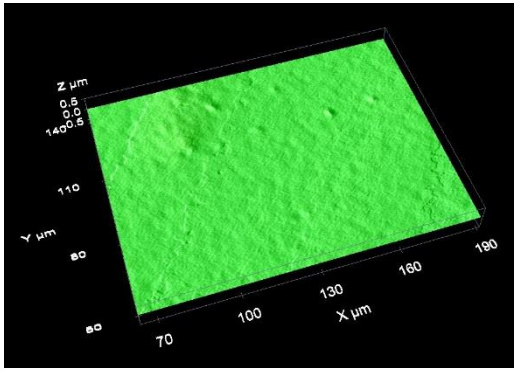
Minimized thickness of ITO (3nm) to keep the sheet resistance high

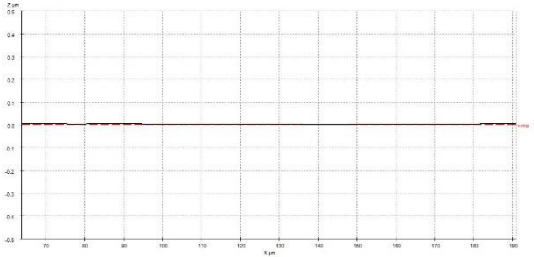
Front junction design to maximize the sheet resistance of the front surface and shunt resistance.

Diamond wire cut vs. polished

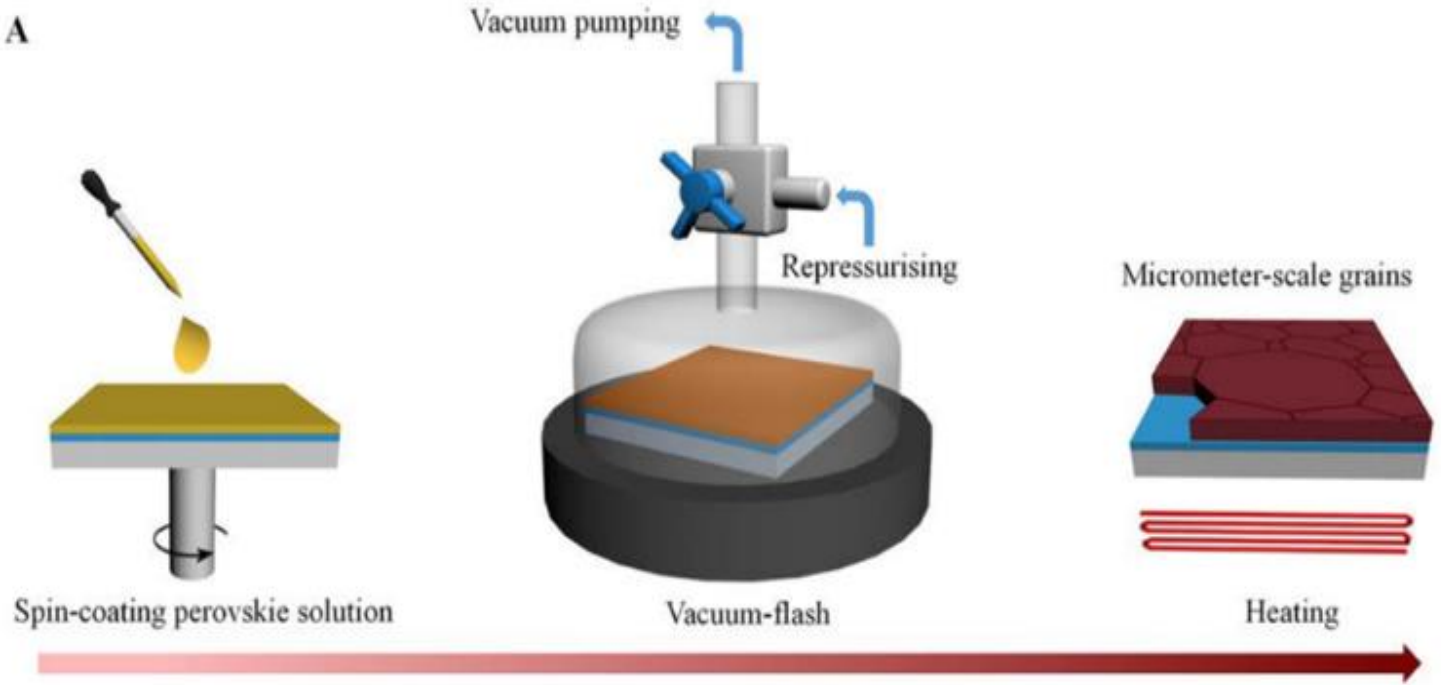






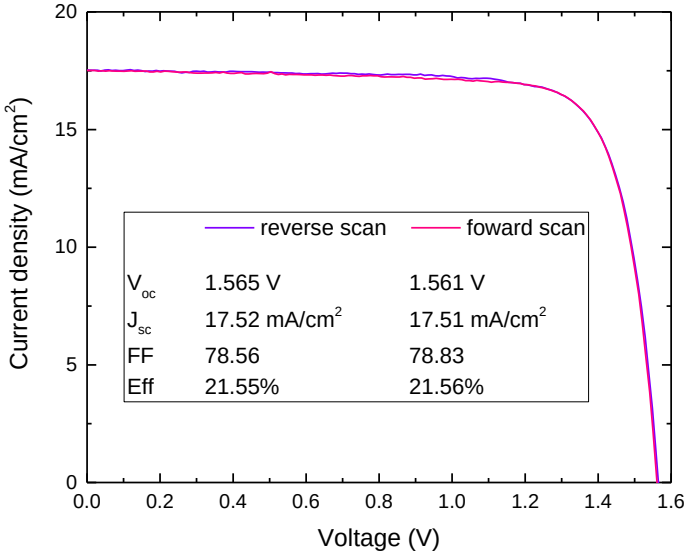


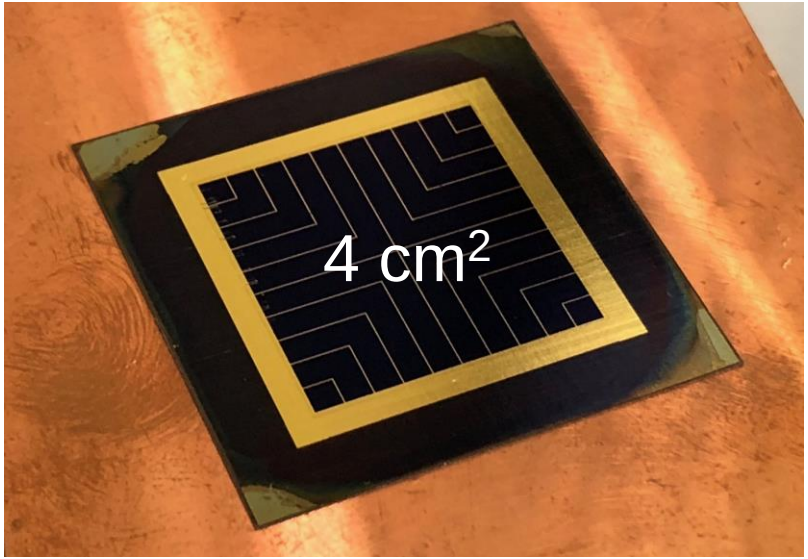
Vacuum-flash process



Li, X.; et a., *Science (80-.).* **2016**, *353* (6294), 58–62.

Device performance





Test report (CSIRO)

Test Report: I-V

PV PERFORMANCE LABORATORY
www.csiro.au

CSIRO

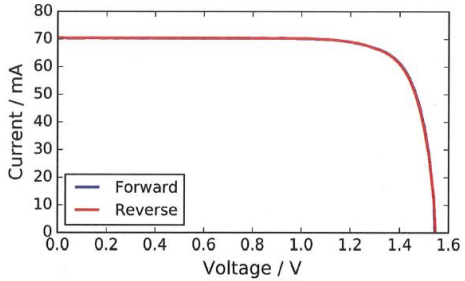
Report Date: 14 June 2019

Australian National University

Test location:
PV Performance Lab
CSIRO Energy Centre
10 Murray Dwyer Cct
Mayfield West NSW
2304 Australia

Customer address:
Ian Ross Building
31 North Road
Acton ACT
2601 Australia

TEST RESULTS : N0024-ANU-D01_001



	Forward	Reverse
Open-circuit voltage:	1.5440 ± 0.0371 V	1.5469 ± 0.0372 V
Short-circuit current:	70.38 ± 3.88 mA	70.49 ± 3.89 mA
Maximum power:	87.81 ± 5.29 mW	87.66 ± 5.28 mW
Fill factor:	80.81 ± 2.80 %	80.40 ± 2.78 %
Efficiency:	21.20 ± 1.28 %	21.16 ± 1.28 %

Results are expressed at Standard Test Conditions (cell temperature 25 °C and spectral irradiance AM1.5G per IEC 60904-3, 1000 W/m^2). Uncertainty values shown are expanded uncertainties expressed with a coverage factor of k=2. The illuminated area was 4.143 ± 0.020 cm^2, as defined by an aperture mask mounted on the cell by the customer.

Conclusion and future work

- Solution processed perovskite sub-cell is deposited on the industrial standard c-Si sub-cell
- 21.2% (certified) is achieved on a 4 cm^2 device
- Optimise the band gap of the perovskite layer (1.53 eV → 1.72 eV) to enhance V_{oc} of the device
- Replace the $FA_{0.3}MA_{0.7}PbI_3$ composition with $Cs_{1-x}FA_xPbI_{1-y}Br_y$ for better stability
- Improve yield through higher shunt resistance

Acknowledgements

Australian National University

Solar JinKO | Building Your Trust in Solar

Tom White
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The Duong
Jun Peng
Daniel Walter
Arafat Mahmud
Naeimeh Mozaffari
Grace Tabi

Xinyu Zhang
Menglei Xu
Jin Hao

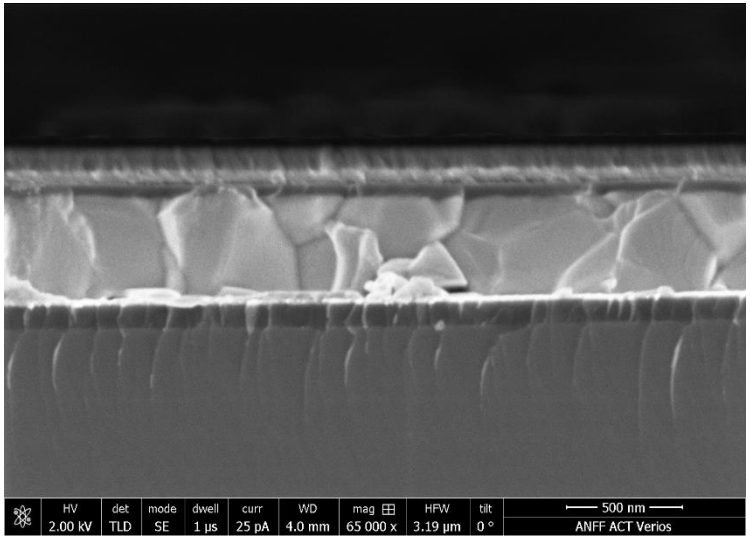

Australian
National
University


Solar
JinKO
Building Your Trust in Solar

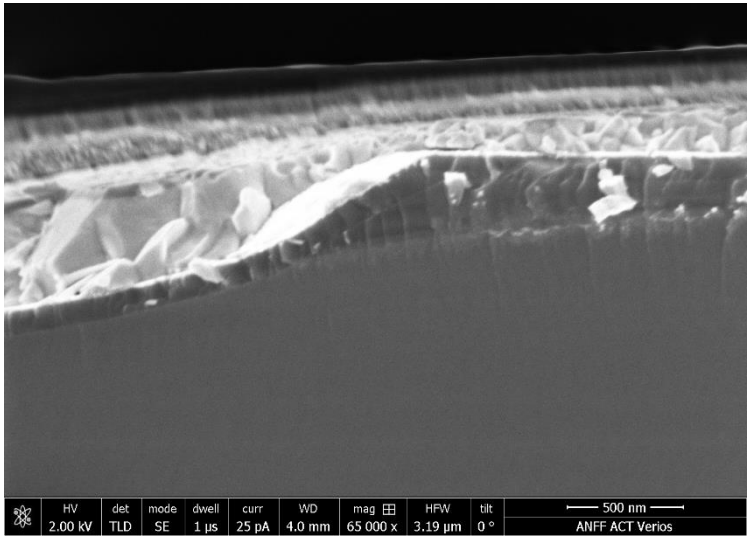

ARENA
Australian Government
Australian Renewable
Energy Agency

THANK YOU!

Cross-section views



flat area of the wafer



on the ridge of the wafer