Impact of Pre-Annealing on Industrially LPCVD Deposited PolySi Hole-selective Contacts

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Abstract: We present the beneficial effect on passivation of industrially LPCVD deposited polySi/SiO_X hole-selective contacts by the introduction of a pre-annealing step prior to the boron diffusion. We investigate the influence of the pre-anneal temperature on passivation quality and crystallinity. A clear increase in passivation quality is observed on planar and textured surfaces as well as for various polySi thicknesses (100 – 230nm) and thermal SiO_X growth temperatures (600 – 800°C). On planar surfaces and without the use of atomic hydrogenation, we report an increase in iV_{OC} of around 5mV with every additional increase of pre-annealing temperature by 50°C (> 900°C) leading to an iV_{OC} of 720mV (J_0 = 9.3fA/cm^2). After atomic hydrogenation, the effect of pre-annealing is less pronounced nevertheless a gain in iV_{OC} (reduction in J_0) of 5-10mV (2-5fA/cm^2) is achieved comparing samples without pre-anneal with samples after a pre-anneal at 1050°C. On textured surfaces on the other hand, the beneficial effect is more pronounced after the atomic hydrogenation and a preannealing at 1050°C leads to an iV_{OC} (J_0) of 705mV (16.8fA/cm2), which is a gain (reduction) by 24mV (21.7fA/cm2) compared to samples without a pre-annealing step.

Introduction: Carrier-selective passivating contacts based on a thin silicon oxide (SiO_X) layer capped by a highly doped polycrystalline silicon (polySi) have achieved impressive results over the last years [1]–[9], including word-record efficiencies in laboratory devices [10], [11], and are currently adopted by manufacturers as next generation for crystalline silicon solar cells [12], [13]. In recent years, the gap between electron-selective n-type contacts and the more challenging hole-selective p-type contacts is closing thanks to the introduction of more sophisticated multilayer systems [9] to control the boron diffusion or by the incorporation of C atoms [6], [14], [15].

In this work, we present another way to achieve high performing hole-selective contacts using a pre-annealing of the intrinsic SiO_X/polySi structures before the boron diffusion takes place. On industrially fabricated symmetrical SiO_X/polySi structures, we present the beneficial effect for a wide range of pre-anneal temperatures.

Experimental: This study was performed on symmetrical test structures using chemically polished and industrially textured 1-5 ohmcm phosphorus doped n-type Cz c-S wafers with a thickness of ~180 µm (textured: ~170 µm). Thermal oxidation at three different temperatures (600°C, 700°C, 800°C) is followed by intrinsic polySi deposition via low-pressure chemical vapour deposition (LPCVD) fabricating three different thicknesses (100nm, 175nm, 230nm). Up to here, the sample fabrication was performed in Jinko Solar in industrial mass-production tools. A pre-annealing was performed using five different temperatures (850°C, 900°C, 950°C, 1000°C, 1050°C) for 60min followed by the same boron diffusion for all samples. After a forming gas anneal (FGA) at 425°C for 30min one sample of each condition went on for atomic hydrogenation via an Al_2O_X:H/SiN_X stack with subsequent annealing at 500°C in FGA, whereas a sister sample was kept for contact resistance measurements.

Results: Figure 1 and Figure 2 depict the passivation quality on planar and textured samples, respectively, as a function of the pre-annealing temperature. In Figure 1a and b, we observe a clear increase in iV_{OC} (decrease in J_0) with increasing pre-annealing temperature independently of the SiO_X growth temperature or the polySi thickness. For pre-annealing temperatures above 900°C, we observe an increase of ~5mV with every additional increase of pre-annealing temperature by 50°C leading to an iV_{OC} of 720mV (J_0 = 9.3fA/cm^2) after FGA. After atomic hydrogenation, a gain in iV_{OC} (reduction in J_0) of 5-10mV (2-5fA/cm^2) is observed comparing samples without pre-anneal and samples after a pre-anneal at 1050°C leading to an excellent passivation with an iV_{OC} of 729mV and a J_0 of 3.1fA/cm^2 using a pre-annealing at 1050°C.

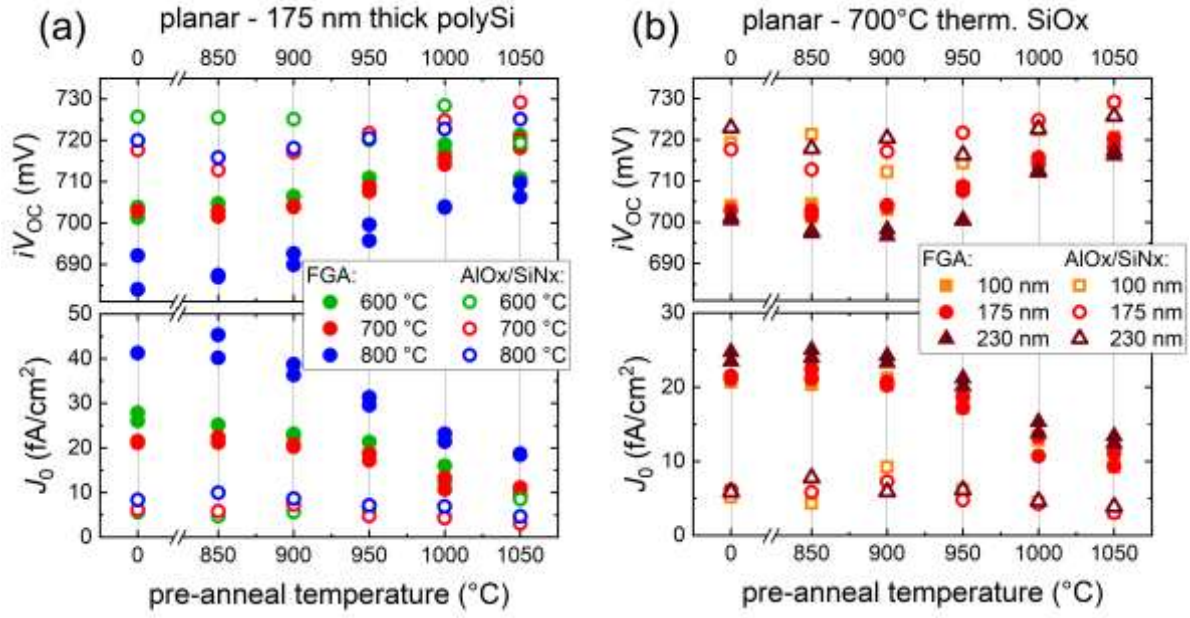

Figure 1: iV_{OC} (top) and J_0 (bottom) for planar samples as a function of pre-annealing temperature measured after FGA (filled symbols) and after atomic hydrogenation via an AlOx/SiNx stack (open symbols). In (a) the thermal SiO_X growth temperature is varied between 600°C (green), 700°C (red) and 800°C (blue) keeping the polySi thickness constant at 175nm. In (b) the polySi thickness is varied between 100nm (orange squares), 175nm (red circles) and 230nm (dark red triangles) for 700°C thermal SiO_X.

As for the planar surfaces, on textured surfaces (Figure 2) an increase in passivation quality is observed with increasing pre-annealing temperature. In general the iV_{OC} (J_0) on textured surfaces is 20-30mV lower (20-30fA/cm^2 higher) than on planar surfaces which is attributed to a poorer passivation ability of the SiO_X layer on (111) surfaces compared to (100) surfaces [16]. An interesting point is that on textured surfaces the beneficial effect of the pre-anneal is more pronounced after the atomic hydrogenation than directly after FGA, which is different than observed on planar surfaces. The optimum with a pre-annealing at 1050°C leads to an iV_{OC} (J_0) of 705mV (16.8fA/cm^2), which is a gain (reduction) by 24mV (21.7fA/cm^2) compared to the 681mV (38.5fA/cm^2) without a pre-annealing step.

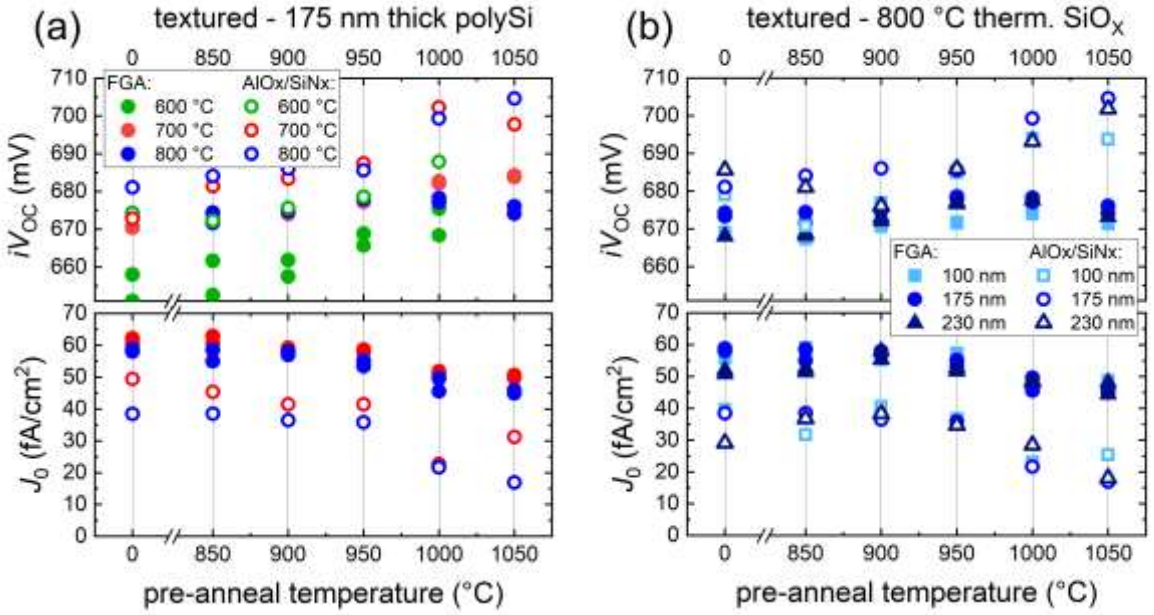

Figure 2: iV_{OC} (top) and J_0 (bottom) for textured samples as a function of pre-annealing temperature measured after FGA (filled symbols) and after atomic hydrogenation via an AlO_X/SiN_X stack (open symbols). In (a) the thermal SiO_X growth temperature is varied between 600°C (green), 700°C (red) and 800°C (blue) keeping the polySi thickness constant at 175nm. In (b) the polySi thickness is varied between 100nm (light blue squares), 175nm (blue circles) and 230nm (dark blue triangles) for 800°C thermal SiO_X.

Contact resistivity measurements were performed using the TLM method [17]. Values for the contact resistivity ρ_C are found between 0.1 – 1 $m\Omega cm^2$ with no clear trend regarding the SiO_X growth temperature, polySi thickness or pre-annealing temperature and are therefore not plotted here.
Electrically active boron profiles are assessed using electrochemical capacitance voltage measurements (ECV) on planar surfaces (Figure 3a). No clear difference is observed for a variation in pre-anneal temperature for the in-diffused profile within the wafer, but a slightly lower boron concentration within the polySi is detected for higher pre-annealing temperature.

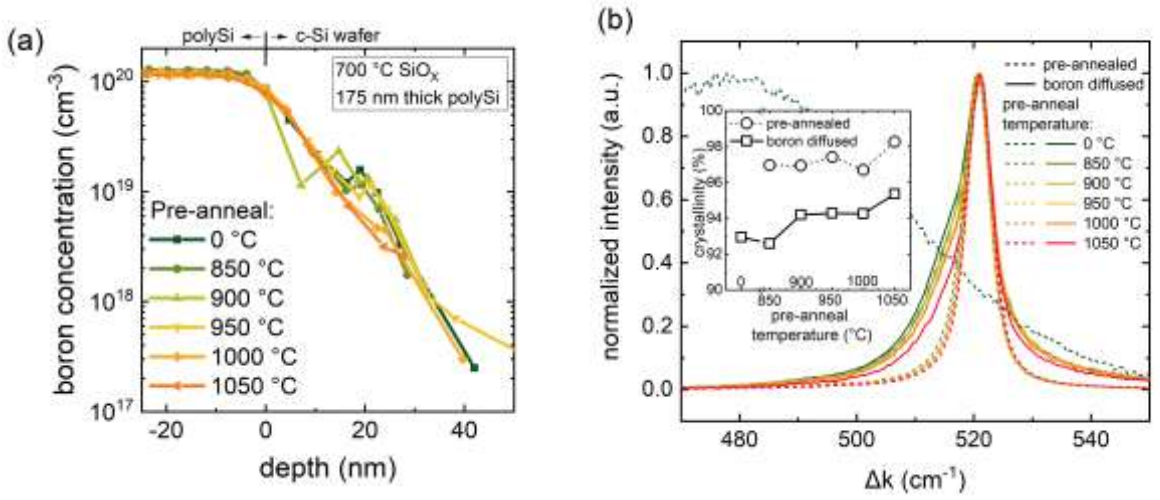

Figure 3: In (a) the active boron doping profiles measured by ECV shown in the region around the interface of polySi/SiO_X/c-Si. The pre-annealing temperature is varied between 0°C (no pre-annealing, dark green) and 1050°C (orange). In (b) normalized Raman spectra before (dotted lines) and after boron diffusion (solid lines) are plotted varying pre-annealing

temperature from 0°C (dark green) up to 1050°C (red) for the case of 175nm thick polySi on 700°C grown SiO_X. The inset in (b) shows the estimated crystallinity.

The crystallization of the polySi layer is assessed using Raman spectroscopy on the planar samples with an excitation wavelength of 442nm (Figure 3b). In the LPCVD grown state (0°C) a broad peak around 480cm^{-1} suggests a completely amorphous film. After pre-anneal, the appearance of a strong peak at 520cm^{-1} indicates crystallisation of the film, and we note that the presence of a small shoulder at 515cm^{-1} decreases with increasing pre-anneal temperature. The crystallinity increases from 96% to 98.3% after pre-anneal at 1050°C (inset Figure 3b). After boron diffusion, the peaks widen and the shoulder gets clearly enhanced as boron atoms cause damage to the crystal structure during the diffusion [18]. This results in a drop in the estimated crystallinity by ~3% ending up at values between 93.0% (no pre-anneal) and 95.4% (1050°C).

Conclusion: We have presented the beneficial effect on passivation of industrially LPCVD deposited polySi/SiO_X hole-selective contacts by the introduction of a pre-annealing step prior to the boron diffusion. Increasing the pre-anneal temperature lead to a higher crystallization of the boron doped polySi layer, while the in-diffusion of dopants to the wafer is not affected. A clear increase in iV_{OC} (decrease in J_0) is observed with increasing pre-annealing temperature independently of the SiO_X growth temperature or polySi thickness. On planar surfaces and after atomic hydrogenation, we observed a gain in iV_{OC} (reduction in J_0) of 5-10mV (2-5fA/cm2) after a pre-anneal at 1050°C leading to an excellent iV_{OC} (729mV) and J_0 (3.1fA/cm^2). On textured surfaces after atomic hydrogenation and a pre-annealing at 1050°C an iV_{OC} (J_0) of 705mV (16.8fA/cm^2) is found, which is a gain (reduction) by 24mV (21.7fA/cm2) compared to samples without a pre-annealing.

Acknowledgement: This work has been supported by the Australian Renewable Energy Agency (ARENA) through project RND016. JS acknowledges support through an Australian Centre for Advanced Photovoltaics (ACAP) postdoctoral fellowship. We owe thanks to the Australian National Fabrication Facility (ANFF) for providing access to some of the facilities used in this work.

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