ASIA-PACIFIC SOLAR RESEARCH CONFERENCE

PEER REVIEWED
ASIA-PACIFIC
SOLAR RESEARCH CONFERENCE

Integrating III-V materials for high performance and novel PV Applications

C. Yi, H. Wang, A. Soeryardi, M. Juhl, Z. Sun, A. Ho-Baillie, S. P. Bremner[1]
[1]*School of Photovoltaic and Renewable Energy Engineering, UNSW Sydney, Kensington 2052, Australia*

Abstract

When the highest performance photovoltaic devices are required the III-V materials system stands apart, delivering the current record performance cells, both in terms of multi-junction and single junction devices. This is inherently due to superior optoelectronic performance stemming from direct band gaps for most of the alloys of interest at required band gaps with modest lattice mismatch between alloys. A further advantage is the demonstrated ability to control and manipulate extended crystalline defects, further broadening the alloys that can be integrated. The high radiative efficiency of III-V materials also makes them attractive for novel applications, that often require the recombination to be exclusively radiative in order to unlock the novel power conversion mechanisms. This paper will look at the use of III-V materials in different applications combined with the industrially ubiquitous silicon. World record results for high performance III-V on silicon multi-junction devices via GaP buffer layers are presented. The integration of III-V material with silicon via the use of strained layer superlattices will also be covered. Some of the future work to be done with both approaches will be covered.

Multi-junction solar cells realised in the III-V materials system have delivered the highest efficiencies reported for photovoltaic devices. The typical lattice matched device has GaInP grown on GaAs(In) with integration on a Germanium substrate, this triad has been expanded by the use of metamorphic buffer layers, where the lattice constant is changed in a manner that controls the density of dislocations formed due to lattice mismatch below the critical value of 10^6 cm^{-2} [1]. Whilst impressive performance has been delivered over decades of research, the key barrier to widespread adoption is the material cost, particularly of the substrate. The incorporation of high performance III-V materials (all III-V solar cells are effectively thin film devices with thicknesses ~2-3 μm) with the industrially ubiquitous silicon is therefore attractive. Fortunately, silicon has the ideal band gap for a double junction device, and the sacrifice in efficiency due to non-ideality of the silicon band gap in triple junction devices is minimal [2]. The major issues for III-V integration with silicon have been lattice mismatch, thermal expansion coefficient mismatch, as well as polar on non-polar growth (anti-phase domains, where the ordering of III cations and V anions in the lattice is confused since the silicon does not provide a good template for growth).

The key breakthrough for III-V on silicon monolithic tandem PV devices was the demonstration of high quality growth of GaP on silicon [3]. This requires the use of silicon deliberately offcut so double atomic monolayer steps are formed on the silicon surface, avoiding anti-phase domains, allowing for much lower crystalline defect density. Lattice mismatch mitigation strategies already developed for III-V materials can then be adapted to produce two or three cell multi-junction devices. Working with our collaborators at Ohio State University, a tandem solar cell consisting of a GaAsP cell on top of a silicon bottom cell with a GaP buffer layer to integrate the III-V material with the silicon has been developed. The motivation for using GaP is two-fold, being a close lattice match to silicon and having a band gap value that would make the buffer effectively transparent in any finished device.

The silicon solar cell in such a device converts a truncated solar spectrum, requiring a modified design [4]. The GaP/Si interface also limits performance, being the front surface for the bottom silicon cell, some of the challenges in this space, including lack of data on this interface will be covered. It will be shown that devices will need to accommodate a relatively high interface recombination rate. Additionally, there have been challenges in terms of preserving the minority carrier lifetime in the silicon, allowing a high-performance device. Early results indicated a catastrophic drop in lifetime that can now be circumvented [5], some insights found in addressing this problem and the solutions being used will be discussed [6].
The latest results for the OSU/UNSW effort are included in Figure 1. This recently confirmed world record performance of 23.4% efficiency under AM1.5G spectrum [7], has improved on the previous mark, also set by OSU/UNSW, by over 3% absolute, reflecting the rapid learning that has taken place. An analysis of where the efficiency losses are and how performance will be improved further in the near future and innovative approaches to contacting [8], will be presented.

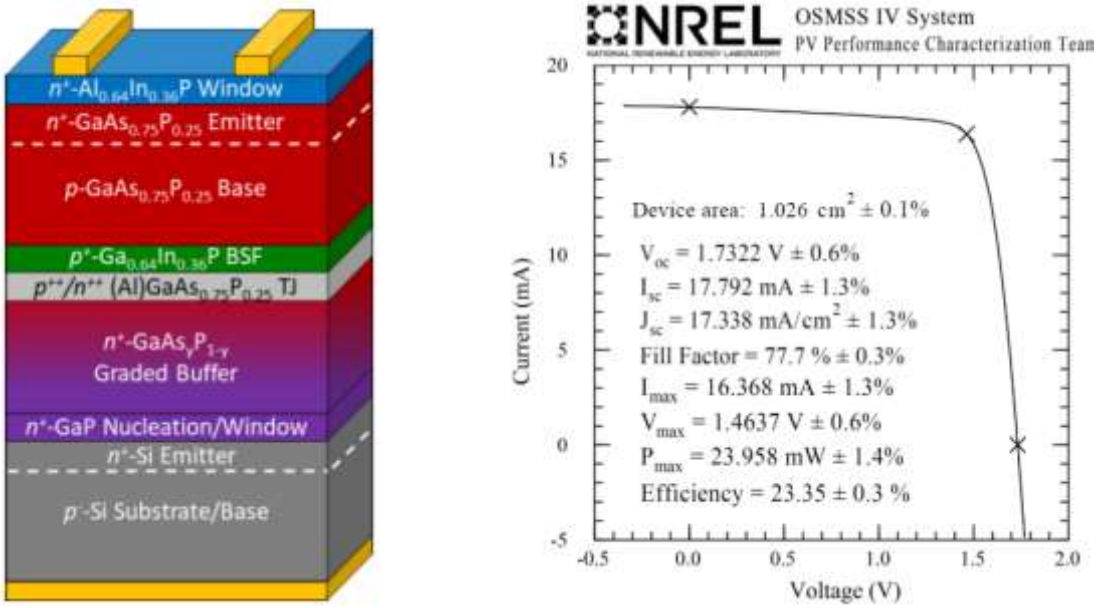

Figure 1: Left; simple layer schematic of OSU/UNSW III-V on Si tandem solar cell, showing most relevant structure information. Right officially certified light I-V measurement provided by NREL, showing a new record performance of 23.4% efficiency.

An alternative to the GaP buffer approach is to directly grow III-V material on silicon with a large lattice mismatch and to then mitigate the extended defects that are formed through strain engineering designs. Recently it has been shown that an initial AlAs layer, grown in an atomic layer or migration enhanced layer by layer mode, can give lower TDDs, due to a lower surface migration length for Al as compared to Ga [9]. The TDDs for the subsequently grown GaAs can be reduced from typically 10^8 cm^{-2} range towards the optoelectronic performance threshold in the 10^6 cm^{-2} range using strained superlattice structures (SLSs).
The SLS approach introduces layers under compressive strain when grown on the GaAs and meaning dislocations, which are extended disruptions to the atomic ordering in the lattice, will move with higher velocity along its glide planes than for an unstrained layer. For III-V materials the glide planes are <111> planes for the most common dislocations, the velocity determined by the glide activation energy (related to band gap), as well as the lattices mechanical properties, through the bulk modulus. The general principle is to anneal the structure in-situ, after growing thin layers of the strained material with GaAs between each layer, then with a thin GaAs layer on top. The anneal step allows dislocations rapid motion along glide planes, and with a relatively high density, dislocations

meet and combine to form edge dislocations parallel to the growth surface, terminating the dislocations. This reduces TDD each time the SLS structure is grown and annealed [10].
The selection of materials to use for the SLSs is not straightforward, since the lattice mismatch needs to be enough to bring about strain, but not so excessive that misfit dislocations localised at the interface are favoured. The band gap can not be too large as this will raise the activation energy for dislocations to move, meaning the anneal temperature will need to be too high. Finally, the lattice must have mechanical properties, like the bulk modulus, that will also ensure good dislocation motion at reasonable anneal temperatures. One such material GaAsSb [11] has been selected using these criteria, a process that will be explained in the final presentation. Results for this materials system, with 5x 5nm GaAsSb layers with 5nm GaAs layers and a 200nm GaAs cap annealed at 660C for 5 minutes has been repeated 4 times. Cross sectional transmission electron microscope images shown in Figure 2, show the clear reduction in TDD in such a sample. Measurements indicate that the final TDD is in the low 10^6 cm^{-2} near the surface of this structure, making it a promising platform for a III-V based solar cell to be grown on top. Further work is ongoing and will be reported on in the final presentation.

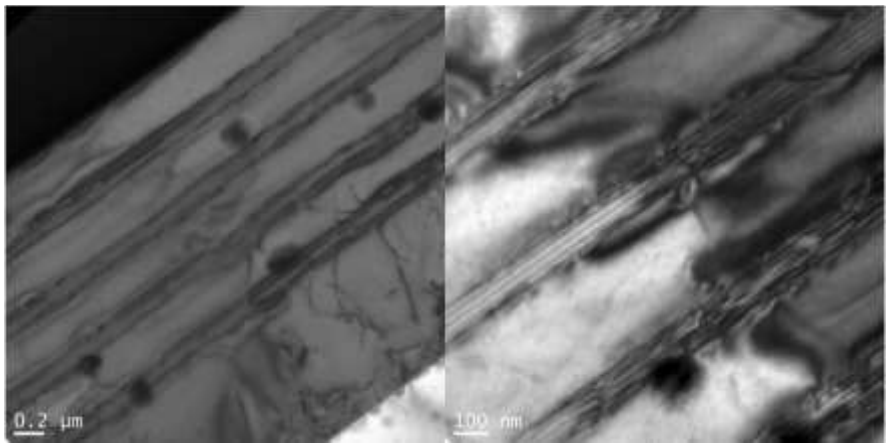

Figure 2: Transmission Electron Microscope bright field images showing extended crystalline defects in a GaAs/GaAsSb strained superlattice structure. After four cycles including a high temperature anneal of the layers after deposition that the density of defects is significantly reduced.

Two different approaches to integrating III-V materials with silicon are presented. The first, using GaP buffer layers, has delivered world record III-V/Si tandem performance. Challenges in developing the high performance silicon bottom cell and scope for improvements will be reviewed. The second, directly integrating GaAs on silicon, with GaAsSb based strained superlattice structures for dislocation density reduction is also presented. Both approaches display the potential for integrating III-V materials to deliver high performance and novel application photovoltaic devices in the near future.

References

[1] C. Andre et al., "Impact of dislocation densities on *n*+/*p* and *p*+/*n* junction GaAs diodes and solar cells on SiGe virtual substrates," *Journal of Applied Physics*, 98, 014502, 2005.
[2] I. Almansouri et al., "Supercharging Silicon Solar Cell Performance by Means of Multijunction Concept," *IEEE Journal of Photovoltaics*, 5(3), 968, 2015.
[3] T. Grassman *et al.*, "Control and elimination of nucleation-related defects in GaP/Si (001) heteroepitaxy," *Applied Physics Letters,* vol. 94(23), 232106, 2009.
[4] I. Almansouri et al., "Designing bottom silicon solar cells for multijunction devices," *IEEE Journal of Photovoltaics*, 5(2), 683, 2014.
[5] C. Zhang et al., "Silicon Nitride Barrier Layers Mitigate Minority-Carrier Lifetime Degradation in Silicon Wafers During Simulated MBE Growth of III–V Layers," *IEEE Journal of Photovoltaics,* 9(2), 431, 2019.

[6] C. Yi et al., "The role of grown-in defects in silicon minority carrier lifetime degradation during thermal treatment in epitaxial growth chambers," *IEEE Journal of Photovoltaics*, submitted.
[7] M. Green et al., "Solar cell efficiency tables (version 56)," Progress in Photovoltaics: Research and Applications, 28, 629, 2020.
[8] N. Western and S. P. Bremner, "Hydrogenation and Gettering Compatible p-Type Contacts for Multicrystalline Silicon Cells, Free of Light, and Elevated Temperature Induced Degradation," *IEEE Journal of Photovoltaics* (accepted).
[9] A. D. Lee, et al., „InAs/GaAs quantum-dot lasers monolithically grown on Si, Ge, and Ge-on-Si substrates," IEEE Journal of Selected Topics in Quantum Electronics, 19, 1901107, 2013.
[10] T. Ward et al., "Design rules for dislocation filters," Journal of Applied Physics, 116(6), 063508, 2014.
[11] Z. Zhang et al., "Sb dissociative surface coverage model for incorporation of antimony in GaAsSb layers grown on GaAs (0 0 1) substrates," *Journal of Crystal Growth*, 526, 125231, 2019.