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Light-Induced Degradation And Recovery In Multicrystalline Silicon: Dependence On Wafer Thickness

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Light- and elevated temperature-induced degradation (LeTID) is a well-known phenomenon that occurs in crystalline silicon (c-Si) wafers and cells. Multiple research groups worldwide have been focussed on examining its cause and developing solutions, owing to its presence in nearly all silicon types [1]–[3] and particularly severe deterioration (up to $16\%_{rel}$. [4]) it can cause in passivated emitter and rear cells (PERCs). Despite the uncertainty about the underlying defect, the empirical trends correlating it with firing temperature [5], [6] and surface passivation layers [7], [8] have narrowed the search of potential candidates involved in LeTID. There is a growing body of literature suggesting the involvement of excess bulk hydrogen [3], [8]–[11]. In this work, we investigate multicrystalline silicon (mc-Si) lifetime test structures of different thicknesses. We report that the extent of degradation reduces with the thickness of the wafer, supporting the findings presented in [12]. However, we find that thinner wafers still suffer from LeTID when fired at sufficiently high temperatures. With similar reaction rates observed in the samples, we explain these findings with a defect model based on the migration of hydrogen during the firing process, i.e. the migration into the bulk during ramp-up and out-diffusion during cool-down.

P-type mc-Si wafers (~190 µm, 1.6 Ω.cm) from neighbouring ingot positions (sister wafers) were selected. All the samples underwent phosphorus gettering diffusion (~60 Ω. sq^{-1}) on both sides. These diffused layers were chemically removed using an HNO_3/HF solution for different times to obtain wafers in the 115-190 µm thickness range. The wafers were then symmetrically passivated with remote plasma-enhanced chemical vapor deposition (r-PECVD) based AlO_x:H/SiN_x:H stacks. The wafers were then fired at peak set temperatures of 775 ºC (actual- 610 °C), 855 ºC (714 °C) and 950 ºC (839 °C) in a fast firing belt furnace (Schmid) at a speed of 450 cm/min. The samples were laser cleaved into 3.9 × 3.9 cm^2 tokens and tested for LeTID at 130 ºC under 44.2 kW/m^2 using a 938 nm laser and 1 kW/m^2 (one sun) illumination using halogen lamps. The surface morphology of the samples was characterised by scanning electron microscopy (SEM, FEI Nova NanoSEM 450).

Results The evolution of the normalised defect concentration (NDD) as a function of time for mc-Si samples fired at a 839 °C and tested at 130 °C under 1 kW/m^2 illumination and high-intensity illumination of 44.2 kW/m^2 is shown in Figure 1.

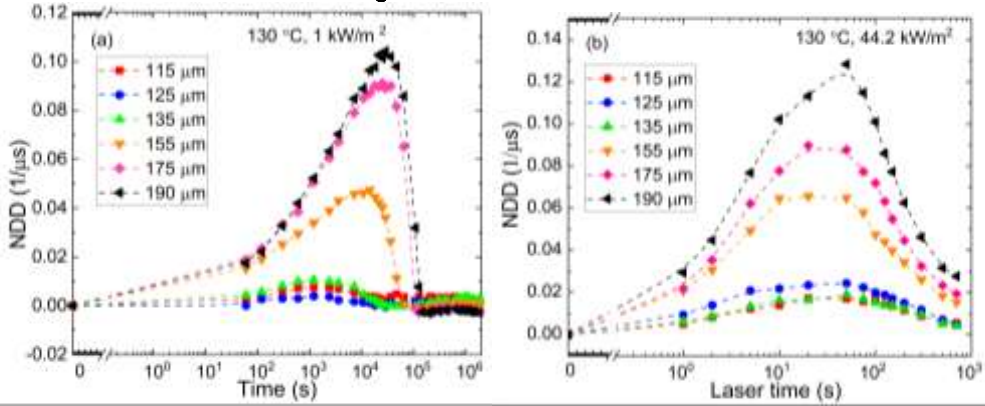
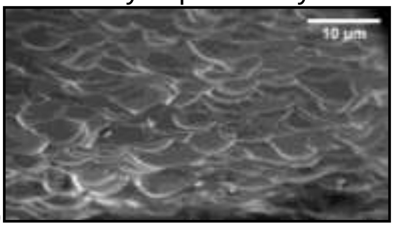


Figure 1. Progression of NDD with time when the samples were tested at 130 ˚C under (a) 1 kW/m^2 illumination using halogen lamps and (c) 44.2 kW/m^2 illumination using laser

In both cases, a positive correlation between wafer thickness and degradation extent was observed. This result is consistent with the results of Bredemeier *et al.* [12]. Despite significant variation in substrate thicknesses, a similar temperature profile (however, lower sample temperature for the thinnest wafer) was observed for all the samples. Hence, thermal history cannot explain the significant variations in NDD. Another interesting observation was the difference in the shape of the graphs, such variation in reaction rates was also reported earlier [13]. The stretched degradation and compressed recovery in case of 1 kW/m^2 [Fig 1(a)] were not found under high illumination intensity [Fig 1(b)]**.** This indicates that the degradation and regeneration rates have a strong Δn dependence and testing at high intensities excludes the differences in Δn within the samples.

Further, to test whether thinner wafers are inherently immune to degradation, identical samples were fired at three different firing temperatures. We observed that the degradation in thicker (190 µm) samples was nearly an order of magnitude higher than the 115 µm samples (not shown here). However, a clear degradation and recovery cycle was observed even in case of 115 µm sample when they were fired at sufficiently high temperatures (839 °C). This is dissimilar to the earlier findings of negligible LeTID in wafers < 120 µm [12]. In addition, we found that the process used for thinning the wafers resulted in a significant variation in surface morphology as shown in Figure 2. The thicker sample [Fig. 2(a)] possess a clear iso-texture (~2.7 µm) in contrast to an almost planar-looking surface in case of the thinnest sample [Fig. 2(b)]. However, the extreme variation in the degradation could not be solely explained by the relatively smaller difference in surface morphology.

(a) 

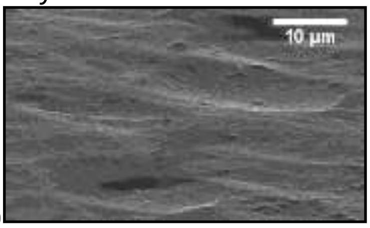
(b) 

Figure 2. SEM images of the mc-Si wafers with a thickness of (a) 190 µm and (b) 115 µm

The NDD data shown in Fig. 1 (b) were fitted using a single exponential decay function as shown in Figure 3. It was found that the extracted rate constants for the degradation and regeneration were nearly identical for all the wafers. This differs from a faster recovery observed in thinner wafers by Bredemeier *et al.* [12] using a diffusion-based model.

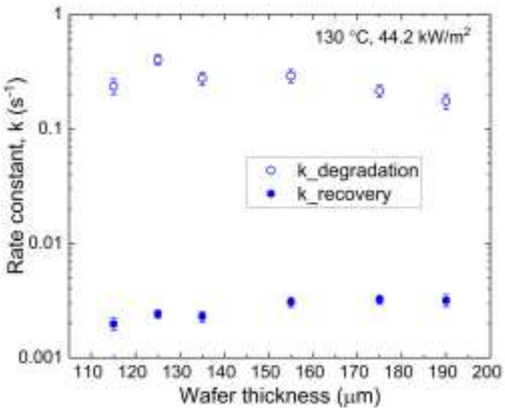


Figure 3. The extracted degradation and recovery rate constants for the samples tested under the illumination of 44.3 kW/m^2 at 130 °C

Considering hydrogen as a plausible defect candidate, an explanation of the reduced $NDD_{max.}$ in thinner wafers lies in the migration of hydrogen during firing. During ramp-up, the amount of hydrogen that in-diffuses into the silicon bulk would likely be similar, owing to the identical dielectric layers in all the samples. However, during cool down, the redistribution of hydrogen would be influenced by the proximity of the surfaces (that work as effective gettering sites) and therefore enhanced out-diffusion of hydrogen is likely in the case of thinner wafers. In addition, hydrogen effusion from the bulk is affected by the total area, it is therefore highly likely that more amount of hydrogen per unit volume out-diffuses from the wafer, leaving the silicon bulk of thinner wafers (with higher surface to bulk ratio) comparitively hydrogen-lean. This can therefore explain the reduced

LeTID extent in thinner wafers. On the other hand, the plausible role of lower concentration of metallic impurities (again due to surface gettering) in thinner wafers cannot be neglected.

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