

## Assessing the material quality of n-type Czochralski silicon wafers grown with melt recharging

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### Abstract

In this study, we explore the electronic properties of industrial n-type silicon wafers grown using the Recharged-Czochralski method (RCZ). This study investigates the effective carrier lifetimes ( $\tau_{eff}$ ), implied voltages at open-circuit condition ( $iV_{oc}$ ) and maximum power point ( $iV_{mpp}$ ) of the samples before and after phosphorus diffusion gettering, indicating the material quality in their as-grown and after-gettered states. Our findings indicate that the as-grown wafers exhibit high material quality, with  $\tau_{eff}$  ranging from 1 ms to 5.5 ms at an injection level of  $5 \times 10^{14} cm^{-3}$  and  $iV_{oc}$  from 740 – 750 mV depending on their solidified fraction within the ingot. After phosphorus diffusion gettering, there was not a significant improvement in  $iV_{oc}$  values throughout the ingots. However, the  $iV_{mpp}$  showed an improvement of approximately 10 mV, particularly towards the tail-end of 4<sup>th</sup> and 7<sup>th</sup> ingots.

### Introduction

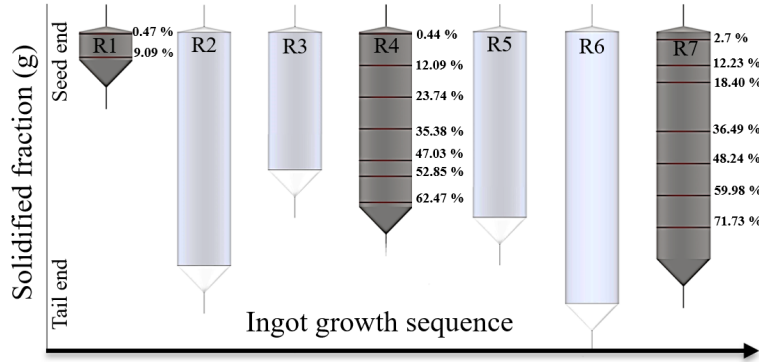
Currently, the silicon photovoltaic (Si-PV) industry has adopted the Recharged-Czochralski (RCZ) method as their standard process for ingot growth. This approach involves periodic replenishment of the melt with polysilicon feedstock materials, enabling the growth of multiple ingots within a single batch [1, 2]. As a result, this process contributes to increasing throughput, maximizing utilization of feedstock material, and leading to a reduction in ingot growth costs. Nevertheless, the feedstock replenishing introduces a risk of potential contamination [3].

Recently, a study on gallium-doped RCZ wafers revealed that melt-recharging indeed increased iron contamination in subsequently grown ingots [4]. Nevertheless, phosphorus diffusion gettering (PDG) significantly reduced the interstitial iron concentration in the wafers. Currently, most high-efficiency solar cell structures, such as Tunnel Oxide Passivated Contact (TOPCon), Polycrystalline silicon on Oxide (POLO), and silicon heterojunction (SHJ) are based on n-type wafers. Consequently, stringent criteria for the minimum carrier lifetime are required for n-type wafers. Therefore, it is essential to investigate the quality of current industrial RCZ ingots to assess their suitability for high-efficiency solar cells.

In this study, we will examine the material quality of n-type RCZ ingots, as indicated by effective lifetimes ( $\tau_{eff}$ ) and implied voltages under the open-circuit conditions (1-sun) ( $iV_{oc}$ ) and at the maximum power point ( $iV_{mpp}$ ). We conduct our study, first on the as-grown wafers, and then we perform PDG to explore any potential changes in material quality.

## Material

The n-type RCZ-Si wafers in this study were provided by Longi Silicon. In this RCZ growth process, seven ingots of varying lengths were grown, amongst them, the first (R1), fourth (R4), and last (R7) ingots were used for the purpose of this study as shown in Figure 1. It is noteworthy that, within the RCZ method, only a segment of the final ingot (characterized by a solidified fraction below 0.7) is conventionally employed for solar cell production, with the remaining section subjected to recycling.



**Figure 1. Schematic of RCZ-Si ingots grown in the same batch. The highlighted ingots are selected in this work and the wafers from different locations are used for assessing the lifetimes are indicated in terms of the solidified fraction (red line).**

## Sample Preparation

The samples for this work were diced from the centre of M10 pseudo-square wafers. All samples were saw-damaged etched by Tetramethylammonium hydroxide (TMAH) solution and RCA cleaned before any further processing. Some of the samples were subjected to the PDG step with phosphorus oxychloride (POCl<sub>3</sub>) vapour diffused at 880 °C for 40 min, resulting in a sheet resistance of 30-40 Ω/□. The diffused layers from the PDG samples were etched by using TMAH solution. Then, all the samples were passivated by silicon nitride (SiN<sub>x</sub>:H) layers using plasma-enhanced chemical vapour deposition (PECVD) method.

$\tau_{eff}$ ,  $iV_{oc}$  at 1 sun light intensity,  $iV_{mpp}$  and wafer resistivity were measured using the quasi-steady state photoconductance and transient photoconductance decay techniques with a WCT-120 tool from Sinton Instruments. The surface recombination velocity (S) attributable to the SiN<sub>x</sub> passivation layers was calculated based on a high-quality n-type float-zone sample (resistivity of 1.8Ω.cm, thickness of 280 μm, and a measured effective lifetime of 18 ms at an excess carrier density ( $\Delta p$ ) of  $5 \times 10^{14} cm^{-3}$ ), via the expression  $\frac{1}{\tau_{eff}} = \frac{1}{\tau_{intrinsic}} + \frac{2S}{W}$ , where  $\tau_{intrinsic}$  is the intrinsic lifetime determined using Niewelt's model [5], and W is the sample thickness.

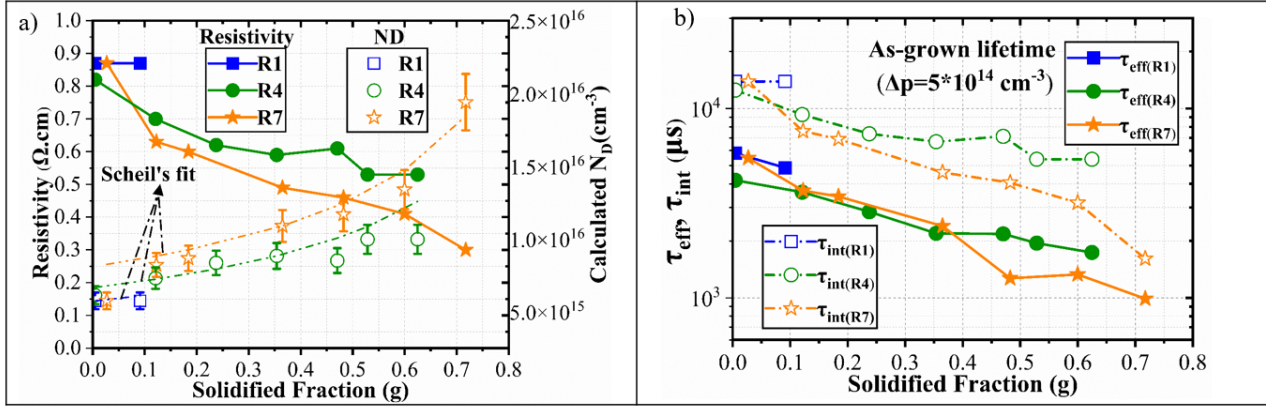
## Results and discussion

### As-grown samples

Figure 2(a) shows that there is a good agreement between the measured doping concentration and Scheil's equation, denoted as,  $C_S = C_0 k_{eff} (1 - g)^{1-k}$ , where  $C_S$  represents the dopant concentration in the ingot at a solidified fraction g,  $C_0$  is the initial concentration of the dopant in the melt, and  $k_{eff}$  is the effective segregation coefficient ( $k_{eff}(P) = 0.35$ ). The error in measured doping concentration is taken as  $\pm 10\%$ , as expected from the uncertainty of dark conductance measurements taken with the Sinton lifetime tester [6].

Figure 2(b) reveals two trends in the measured carrier lifetimes of the selected ingots. Firstly, within a given ingot, there is a discernible decline in carrier lifetime from the seed-end to the tail-end, similar to the intrinsic lifetimes. This phenomenon can be predominantly ascribed to the increasing dopant

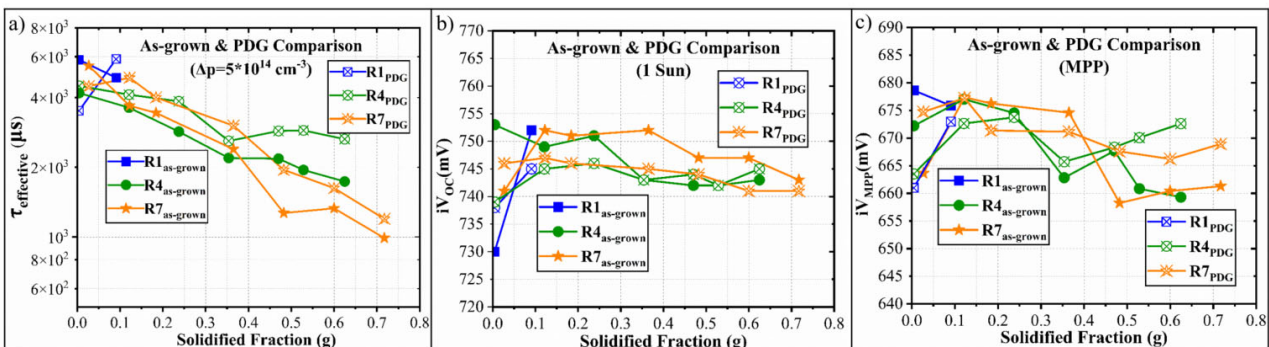
concentration [5], as illustrated in Figure 2(b). Secondly, we observed slightly lower carrier lifetimes in subsequently grown ingots. This reduction in carrier lifetimes is potentially due to the accumulation of impurities within the residual melt after each melt recharging.



**Figure 2. (a) Resistivity and dopant concentration as a function of solidified fraction of the as-grown samples for three RCZ (R1, R4, and R7) ingots (b) Comparison of the measured effective lifetimes and intrinsic lifetimes of the selected ingots at an excess carrier density of  $\Delta p = 5 \times 10^{14} cm^{-3}$ .**

### Impact of phosphorus diffusion gettering

It is well known that doped poly-Si contacts inherently provide gettering effects, thereby alleviating the deleterious effects of impurities within the wafers [7]. It is noteworthy that SHJ solar cells are progressively incorporating pre-gettering steps to enhance the quality of n-type cells. Consequently, this study investigates the impact of PDG on the  $\tau_{eff}$ ,  $iV_{oc}$  at 1 sun light intensity and  $iV_{mpp}$ , as shown in Figure 3. There was a slight improvement in the  $\tau_{eff}$  of the R4 and R7 after PDG; however, considering the voltages, two clear trends were observed: 1) there was no significant improvement of  $iV_{oc}$ , but the obvious gain of 5 – 10 mV was obtained in  $iV_{mpp}$  at the tail of ingots. Furthermore, while the  $\tau_{eff}$  distribution shows expected dependencies on the solidified fraction, the  $iV_{oc}$  shows a weak dependence on ingot position ( $745 \pm 10 mV$ ), suggesting that all of these RCZ grown ingots have good material quality and can be suitable for TOPCon solar cells, and also SHJ cells, perhaps with a pre-gettering step for tail wafers.



**Figure 3. Comparison of (a) the measured effective lifetime of the R1, R4, and R7 ingots at an excess carrier density of  $\Delta p = 5 \times 10^{14} cm^{-3}$  (b)  $iV_{oc}$  at one sun condition and (c)  $iV_{mp}$ .**

## Conclusion

The experimental investigations presented in this study reveal that the industrial n-type RCZ silicon wafers supplied by Longi exhibit high material quality in their as-grown state ( $iV_{oc} = 740 - 750 \text{ mV}$  and  $iV_{mpp} = 670 - 680 \text{ mV}$ ). After PDG process, there were some improvements in carrier lifetime and  $iV_{mpp}$ , of around  $1 \text{ ms}$  and  $10 \text{ mV}$  respectively, suggesting these wafers also benefit from the gettering process provided by standard TOPCon processes, or with a pre-gettering step for heterojunction cells.

## Acknowledgement

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