

Electroplated Copper Metal Contact for GaAs Solar Cells

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Abstract

Copper (Cu) contacts applied to Gallium Arsenide (GaAs) have attracted increasing attention in the realm of cost-effective, high-efficiency solar cell devices. Prior research has underscored the efficacy of Pd/Ge/Cu and Pt/Ti/Pt/Cu evaporated contact configurations, revealing specific contact resistivities ranging from $10^{-5} \Omega\text{cm}^2$. In this work, we explore an alternative deposition method utilizing Cu plating. A specialized barrier system Pd/Ge/Pd/Ni was devised to facilitate the deposition of thick Cu contacts, preventing the formation of voids in n-type GaAs. The results of this study indicate that the contact resistance of plated contacts is comparable to or even lower than that of the reference evaporated contact structure. This highlights the potential of Cu-plated electrodes to achieve contact resistivities as low as or lower than those attained with

h Cu-evaporated electrodes.

1 Introduction

Metal deposition of the front emitter contact of III-V solar cells is a crucial phase in solar cell manufacturing. The design of the front contact involves not only minimisation of the metal resistance, but the overall reduction of losses associated with the front contact, including resistive loss in the emitter, resistive loss in the metal and shading losses. Thick metal and a short distance between fingers can benefit to low metal resistance and low emitter resistive losses, but the presence of metal can prevent light from entering solar cells causing shading losses. In consideration of this trade off, narrow fingers with a high metal height-to-width aspect ratio are desirable.

When working under high concentrations, in order to maximise light capture and maintain a low series resistance, high aspect ratio metallisation with high conductivity becomes even more critical. Typically, III-V cells designed to operate under concentration use Au-based contacts with a thickness of about $5 \mu\text{m}$ [1, 2] due to Au's high conductivity and its ability to form electrical contacts to the GaAs surface contact layer.

However, Au is one of the most expensive metals, following other precious metals rhodium (Rh) and iridium (Ir) [3]. Furthermore, Au deposition on solar cells typically uses evaporation under high vacuum condition, leading to an increase in the fabrication costs and process time due to pumping. Such Au deposition process can cause a significant amount of material wastage due to the excessive usage of metal source during the metal melting process and indiscriminate deposition on all surfaces of the vacuum chamber. Therefore, it is highly beneficial from a cost perspective to develop a targeted deposition method which is both fast and low-cost to replace the current Au deposition whilst maintaining high aspect ratio, low series resistance and low contact resistance. Replacing evaporated Au contacts with plated Cu contacts can potentially resolve the challenges of high costs and long process presented in the conventional III-V solar cell metallisation process.

Our previous work described the development of a barrier system for Cu on GaAs surfaces thereby satisfying the requirement of a low contact resistance [4]. This work continues to document the development of a plated Cu process for the front surface metallisation of III-V solar cells with GaAs as the contact layer. Although the process was developed using epitaxial GaAs precursor wafers with GaAs as a contact, the developed metallisation method has also been applied to other III-V solar cells (1 sun or under concentration).

2 Copper Plating

Metal plating involves an electrochemical deposition of metals from a solution containing metal ions. Copper electroplating is a straightforward process wherein a wafer is immersed in an electrolyte with an applied current and thus Cu ions can migrate and be deposited onto the conductive areas of the wafer regions that are exposed to the electrolyte. In this subsection, the setup and characterisation of the plating process is explained.

To carry out Cu plating, the setup shown in Figure 1 was employed. This setup comprised the following components: an electrolyte, a cathode, a sample holder system, and a current source. The electrolyte used for this setup was Helios Cu plating solution (MacDermid Inc.) [5], a ready-to-use S-based solution designed for solar cells. A phosphorus-doped Cu anode for use in acid Cu plating was used for cathode in this work. The addition of phosphorus could prevent slime formation by incorporating the cuprous ion to form monovalent copper compounds according to [6]. The anode was placed at the bottom of the plating container about 4 cm from the cell surface for electrical connection. The sample was held on the sample holder via vacuum. An aluminium foil was taped on the plastic sample holder that was underneath the solar cell to provide a place for the connection of the current source. In addition, tapes were used on the edges of the sample to prevent the side of the sample from coming into contact with the solution, and this is to prevent possibility of shunting. Once the cell was placed on the holder, the level of the plating solution was adjusted to be slightly above the cell surface. Due to the surface tension of the plating electrolyte, the solution could wet the exposed surface of the cell whilst keeping the back surface dry, and this enables single-side plating. A current source was used as plating rate control in electroplating. The anode of the current source is connected to the Cu electrode and the cathode is connected to the aluminium foil on the sample holder. During the plating process, a direct current was applied to the cell, allowing the Cu in the anode to dissolve into the electrolyte through oxidation and then losing electrons and ionising into Cu cations. The Cu cations formed coordination complexes with the salts in the electrolyte, after which they were transported from the anode to the cathode as demonstrated in Figure 1. At the cathode, the Cu ions were reduced to metallic Cu, resulting in a thin and solid film of Cu deposited on the surface of the cell.

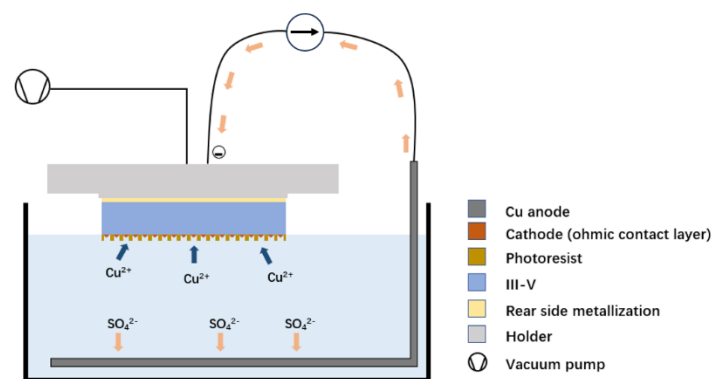


Figure 1 Electrochemical characterisation setup used with the copper plating solution.

3 Voids Control

The Cu-plated contacts were fabricated as shown in Figure 2 (a). After the void-free sample underwent thermal annealing at 300°C for 1 min, voids were generated at the Au/Cu interface and the interface between the seed layers and the Cu layer on n-GaAs samples as shown in Figure 2 (b-d). The void density was found to depend on the thickness of the upper Cu layer. These voids led to poor electrode adhesion and lower contact performance. For the metal finger with a height of $5\ \mu\text{m}$, the contact resistance was increased to the range of $10^{-2}\ \Omega\ \text{cm}^2$ comparing to the value of evaporated contacts in the range of $10^{-5}\ \Omega\ \text{cm}^2$.

Considering the Cu diffusion mechanisms, one possible reason for this void formation is due to defects such as dislocations, twins and grain boundaries that provide a fast route for Cu diffusion [7]. This is prevalent in films deposited by physical vapour deposition processes or electroplating, as they have fine grain structures and columnar grain boundaries [8]. Temperature has a significant effect on defect diffusion due to the thermal energy changes of atoms and molecules in the material [9]. Additional cleaning processes such as wet chemical cleaning and plasma etching cleaning were considered, but the voids still appeared after annealing. Also, an additional Pd layer with a thickness of 20 nm was applied to avoid Ge oxide effects, but no improvement was observed after annealing.

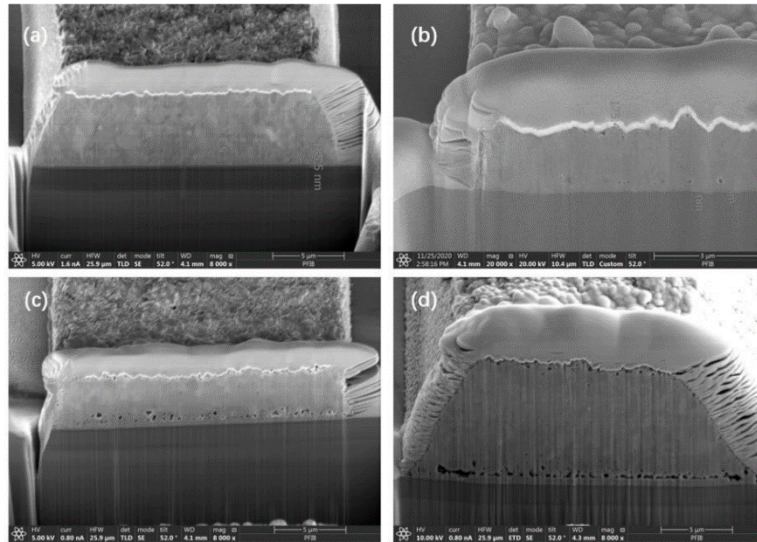


Figure 2 Cross-sectional SEM images for Cu plated fingers at as-deposited condition (a) and after annealing at 300°C for 1 min with different finger heights 1.5 μm (b), 3 μm (c) and 5 μm (d).

The other possible reason is a phenomenon known as Kirkendall effect. The Kirkendall effect is a diffusion-induced phenomenon that can occur at the interface between two materials with different diffusion coefficient [10]. The diffusion coefficient of Cu atoms can be larger than that of Au and Ge atoms during annealing, leading to the formation of a diffusion zone [11]. The excess vacancies could remain in the Cu lattice and could condense to form Kirkendall voids. Nickel was reported to be a solution to avoid such void formation as its diffusion rate is closer to that of Cu and hence an addition of Ni could affect the formation of voids by changing the unbalanced diffusion [12]. This in turn reduces the likelihood of Kirkendall voids forming at the interface.

A thin Ni layer with a thickness of about 200 nm was plated before Cu plating and evaporated before cap layer deposition as shown in Figure 3. The sample underwent thermal annealing at 300°C for 1 min, and no voids were found.

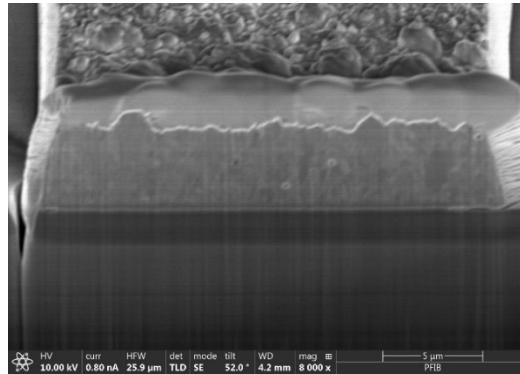


Figure 3 Cross-sectional image for Cu plated finger with extra Ni plated layer between seed layers and Cu layers after annealing at 300°C for 1 min.

4 Specific Contact Resistance for Cu-plated Contacts

The samples used were MBE-grown highly doped n-GaAs (carrier concentration $> 10^{18} \text{ cm}^{-3}$) and p-GaAs (carrier concentration $> 5 \times 10^{18} \text{ cm}^{-3}$) on GaAs substrates. The specific contact resistance of plated contacts and evaporated contacts on both n-type GaAs and p-type GaAs after annealing at 300°C for 1 min are shown in Figure 4. The low specific contact resistance of plated contacts can be obtained for both structures. The specific contact resistance was $(1.9 \pm 0.2) \times 10^{-5} \Omega \text{ cm}^2$ for Pd 10 nm/Ge 150 nm/Pd 10 nm/plated Ni 200 nm/plated Cu 1500 nm/Ni 10nm/Au 100nm on the n-type GaAs substrate. Ni penetration can help prevent the formation of Kirkendall voids then further reduce the contact resistance. The plated Cu contact resistance of p-GaAs samples with a thickness of 1500 nm was measured as $(7.0 \pm 0.9) \times 10^{-5} \Omega \text{ cm}^2$. Contact resistivities of the plated Cu contacts deposited on n-GaAs and p-GaAs were observed to be similar to or lower than the evaporated contacts with the same structure but thin Cu layer (Pd 10 nm/Ge 150 nm/Pd 10 nm/plated Ni 20 nm/plated Cu 150 nm/Ni 10nm/Au 100nm) as shown in Figure 4. This demonstrates that Cu-plated electrodes can achieve contact resistivities as low or lower than that of Cu-evaporated electrodes.

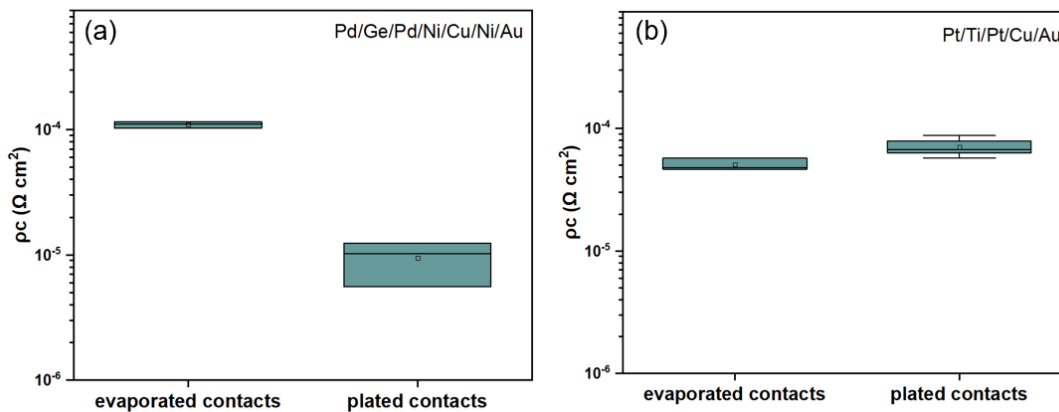


Figure 4 Specific contact resistivities for evaporated and plated ohmic contacts after annealing at 300°C for 1 min on n-GaAs (a) and p-GaAs (b).

5 Conclusion

This work details the Cu-plated front contact process for GaAs-based III-V solar cells. However, voids are commonly formed in n-type GaAs samples after annealing due to the unbalanced diffusion rates between Cu and adjacent metals Ge and Au. To eliminate voids, a thin Ni layer was added before Cu plating as a strategy. Nickel quickly diffused in Cu at high temperature, reducing Kirkendall effects and filling voids. Plating Ni was therefore carried out prior to Cu deposition to

also prevent Ni oxidation. The specific contact resistance of plated contacts for the optimised structure was measured as $(1.9 \pm 0.2) \times 10^{-5} \Omega \text{ cm}^2$ for n-type GaAs with a contact structure of Pd /Ge /Pd /plated Ni /plated Cu/ Ni/ Au after annealing at 300°C for 1 min. For p-type GaAs, the specific contact resistance for the plated Cu contacts using a Pt /Ti /Pt /Cu /Ni /Au layer stack was measured as $(7.0 \pm 0.9) \times 10^{-5} \Omega \text{ cm}^2$. Both values were found similar to or lower than those of the comparative evaporated contact structure, demonstrating that Cu-plated electrodes can achieve contact resistivities as low as or lower than Cu-evaporated electrodes.

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